NETLIST

Datasheet
microSDvault™ SD
128MB to 8GB
NLUSabcdef-pqrstuvwxyz

1. Overview

The Netlist microSD Card is a reliable high capacity media in the industry standard form factor. Available in 128MB to 8GB storage capacities. It is built with Industrial temperature grade SLC NAND Flash technology.

Suitable for embedded industrial applications, it is also used very extensively as storage device for mobile applications, PDAs, portable computers, and other computer applications.

1.1. System Concept

The microSD Memory Card provides application designers with a low cost mass storage device, implemented as a removable card that supports a high security level for content protection and a compact, easy-to-implement interface. microSD Memory Cards can be grouped into several card classes that differ in the functions they provide (given by the subset of microSD Memory Card system commands).

A microSD Memory Card system includes the microSD Memory Card (or several cards) the bus and their Host/Application. The Host and Application specification is beyond the scope of this document. The following sections provide an overview of the card, bus topology, and communication protocols of the microSD Memory Card system. The content protection (security) system description is given in "microSD Memory Card Security Specification" document.

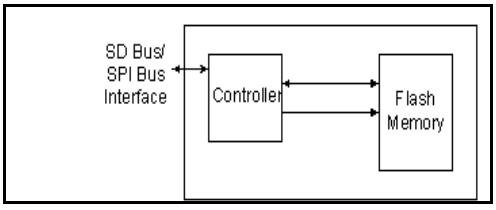
1.2. System Function

- Protecting the chip
- Easy handling for the end user
- Reliable electrical interconnection
- Bearing textual information and image

2. Features

- 128MB to 8GB Memory capacity
- Industrial Temperature Grade - SLC NAND
- Standard Capacity microSD Memory Card: Up to and including 2GB
- High Capacity microSD Memory Card: Up to 8GB
- Dual Voltage microSD Memory Card
    - Standard voltage operation: 2.7- 3.6V
    - Low voltage operation: 1.6 - 3.6V
- microSD class 10 compatible
- Designed for read-only and read/write cards.
- Default mode: Variable clock rate 0-25Mhz, up to 12.5MB/sec interface speed (using 4 parallel data lines)
- High-Speed mode: Variable clock rate 0-50 MHz, up to 25 MB/sec interface speed (using 4 parallel data lines)
- Switch function command supports High-Speed, eCommerce, and future functionality
- Integrated BCH ECC engine
- Contact Protection Mechanism – Complies with highest security level of SDMI standard
- Password Protection of cards (CMD42–LOCK-UNLOCK)
- Built-in write protection features (permanent and temporary) using mechanical switch
- Card Detection (Insert/Remove)
- Protocol attributes of the communication channel:
    - SD Memory Card Communication Channel
    - Six-wire communication channel (clock, command, 4 data lines)
    - Error-protected data transfer
    - Single or Multiple block oriented data transfer

Figure 1: microSD Card Block Diagram



3. Ordering Information

128MB to 8GB microSDvault™ SD
Part Number:
NLUSabcdef-pqrstuvwxyz

Density	Part Number
128MB	NLUS012def-pqrstuvwxyz
256MB	NLUS025def-pqrstuvwxyz
512MB	NLUS051def-pqrstuvwxyz
1GB	NLUS01Gdef-pqrstuvwxyz
2GB	NLUS02Gdef-pqrstuvwxyz
4GB	NLUS04Gdef-pqrstuvwxyz
8GB	NLUS08Gdef-pqrstuvwxyz

4. Part Number Decoder

N	L	U	S	*a*	*b*	*c*	*d*	*e*	*f*	-	*p*	*q*	*r*	*s*	*t*	*u*	*v*	*w*	*x*	*y*	*z*
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

Position	Property	Definitions	
1,2	Netlist Code	NL = Netlist	
3,4	Product Type	US = MicroSDvault™	
5,6,7	Memory Capacity	012 = 128MB 025 = 256MB 051 = 512MB 01G = 1GB	02G = 2GB 04G = 4GB 08G = 8GB
8	Feature Set A	1 = SD1.1 when 9 = 1 2 = SD2.0 when 9 = 0 3 = SD3.0 when 9 = 0	
9	Feature Set B	1 = SD1.1 when 8 = 1 0 = SD2.0 when 8 = 2 0 = SD3.0 when 8= 3	
10	Temperature Range	I = Industrial (-40°C to +85°C)	C = Commercial (0°C to +70°C)
11	"-"	-	
12	Flash Controller	0 = PS7000 1 = S4 2 = S6 3 = SM2682 4 = SM2681 5 = SM2683 6 = SKYMEDI 7 = PS8006	8 = TBD 9 = PS8032 A = PS8035 B = AU7656R C = SM2702AC D = PS8009 E = PS8007 F = SM2702
13	Flash Manufacturer	S = Samsung M = Micron T = Toshiba	H = Hynix 5 = Spansion
14	Flash Type	S = SLC	M = MLC
15	Mount	H = Horizontal	V = Vertical
16,17	OEM Code	AA = Standard Product	
18	Flash Die Geometry	4 = 4x nm 3 = 3x nm	2 = 2x nm 1 = 1x nm
19	Number of CE per Flash Location	1 = 1 CE per Flash Location 2 = 2 CE per Flash Location	4 = 4 CE per Flash Location 8 = 8 CE per Flash Location
20	Number of Flash Location(s)	1 = 1 Flash Location 2 = 2 Flash Locations	4 = 4 Flash Locations 8 = 8 Flash Locations
21	Number of Die per Flash Location	1 = 1 Die per Flash Location 2 = 2 Die per Flash Location	4 = 4 Die per Flash Location 8 = 8 Die per Flash Location
22	Special Feature	0 = None (Standard Product)	

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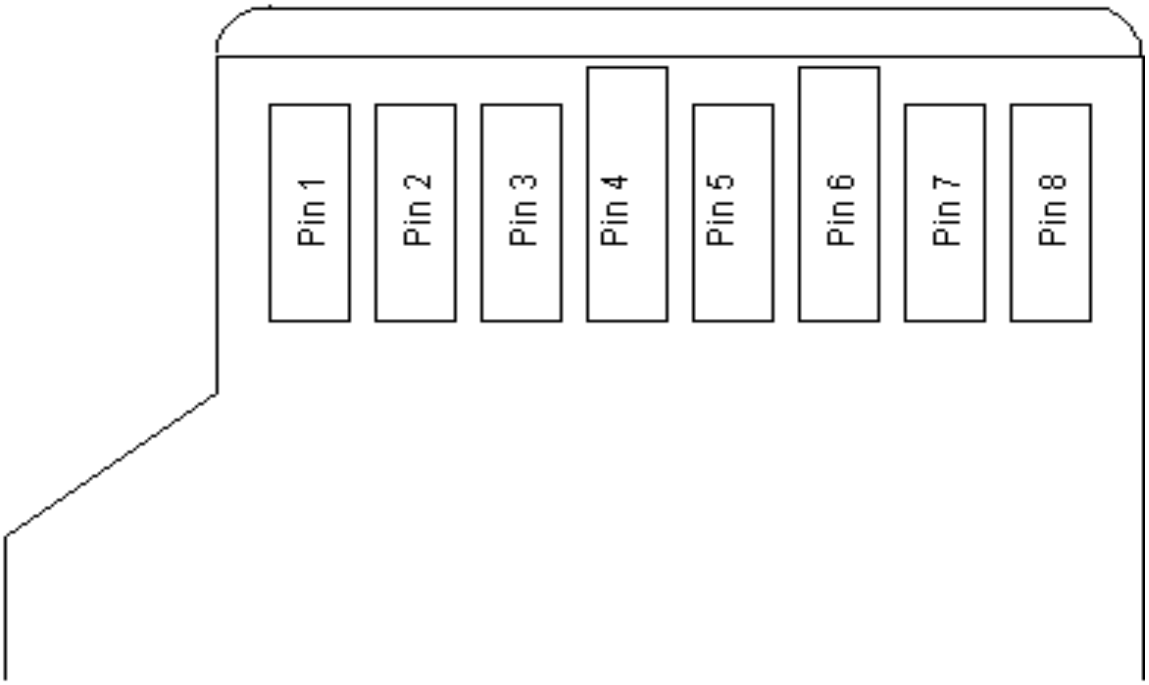
5. Block Diagram



Pin #	microSD Mode			SPI Mode		
	Name	Type1	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [Bit2]	RSV		
2	CD/DAT3	I/O/PP	Card Detect/Data Line [Bit3]	CS	I	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data in
4	V_{DD}	S	Supply Voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply Voltage Ground	Vss	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		

6. Read/Write Property

In terms of read-write property, two types of microSD Memory Cards are defined:

- One Time Programmable (OTP)
- Multiple Time Programmable (MTP)

These cards are typically sold as blank (empty) media and are used for mass data storage, end user video, audio, or digital image recording Read Only Memory (ROM) card. These cards are manufactured with fixed data content. They are typically used as a distribution media for software, audio, video etc.

7. Card Capacity[1] [2]

In terms of capacity, two types of microSD Memory Cards are defined:

Standard Capacity microSD: Supports capacities up to and including 2G bytes (2^{31} bytes). All versions of the Physical Specifications define the Standard Capacity microSD Memory Card.

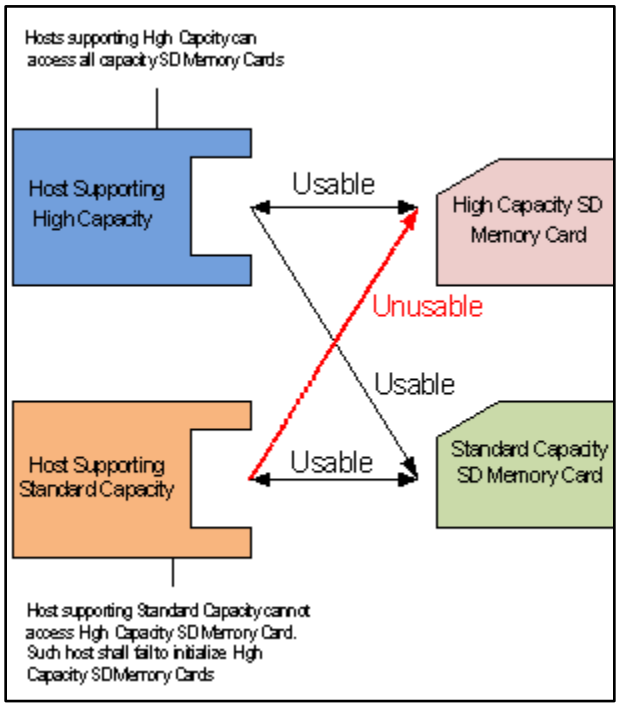
High Capacity microSD: Supports capacities more than 2G bytes (2^{31} bytes). This version of specification limits capacity up to and including 32GB. High Capacity microSD Memory Card is newly defined from the Physical Layer Specification Version 2.00.

Only hosts that are compliant to the Physical Layer Specification version 2.00 or higher and the microSD File System Specification Ver 2.00 can access High Capacity microSD Memory Cards. Other hosts fail to initialize High Capacity microSD Memory Cards.

[1] The Part 1 Physical Layer Specification Version 2.00 and Part 2 File System Specification Version 2.00 allow Standard Capacity microSD Memory Cards to have capacity up to and including 2 GB and High Capacity microSD Memory Cards to have capacity up to and including 32 GB. microSD Memory Cards with a capacity greater than 32 GB will be available with updated versions of Part 1 and Part 2 Specifications.

[2] Hosts that can access (read and/or write) microSD Memory Cards with a capacity greater than 2 GB and up to and including 32 GB, shall also be able to access microSD Memory Cards with a capacity of 2 GB or less.

Figure 2: Host-Cards Usability



Two types of High Capacity microSD Memory Card are specified.

- **Type A** (Single State Card) has single High Capacity memory area. Details of Type A are specified in the Physical Layer Specification version 2.00.
- **Type B** (Dual State Card) has both High Capacity memory area and Standard Capacity memory area. In Type B card, only one memory area can be used at any given time. A mechanical switch is used to select the desired memory area. Details of Type B will be defined in future specifications. It is not necessary for the host to distinguish card types.

8. Speed Class

Five Speed Classes are defined and indicate minimum performance of the cards:

- Class 0 - This class does not specify performance. It includes all the legacy cards prior to this specification, regardless of its performance.
- Class 2 - Are more than or equal to 2 MB/sec performance.
- Class 4 - Are more than or equal to 4 MB/sec performance.
- Class 6 - Are more than or equal to 6 MB/sec performance.
- Class10 - Are more than or equal to 10 MB/sec performance.

Table 1: Speed[3]

<512MB Class 6		1GB Class 6		2GB Class 10		4GB Class 10		8GB Class 10		Units
Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	MB/s[4]
17.88	6.41	17.50	9.58	17.88	12.05	17.28	12.52	17.7	12.5	

9. Command Systems

The microSD commands CMD34-37, CMD50, and CMD57 are reserved for microSD command system expansion via the switch command. Switching between the various functions of the command system function group will change the interpretation and associated bus transaction (i.e. command without data transfer, single block read, multiple block write, etc.) of these commands. Supporting Command system is optional:

- When the 'standard command set' (default function 0x0) is selected, these commands will not be recognized by the card and will be considered as illegal commands (as defined in Version 1.01 of the microSD Physical Layer Specification)
- When the 'vendor specific' (function 0xE) is selected, the behaviors of these commands are vendor specific. They are not defined by this standard and may change for different card vendors.
- When the 'mobile e-commerce' (function 0x1) is selected, the behavior of these commands is governed by the microSD Specifications Part A1: Mobile Commerce Extension Specification.

When either of these extensions is used, special care should be given to proper selection of the command set function, otherwise, the host command may be interpreted incorrectly.

All other commands of the microSD memory card (not reserved for the switch commands) are always available and will be executed as defined in this document regardless of the currently selected commands set.

[3] Speed is based on empty card.

[4] The unit of performance [MB/sec] indicates 1000x1000 [Byte/sec] while the unit of data size [MB] indicates 1024x1024 [Byte]. This is because the maximum microSD Bus speed is specified by the maximum microSD clock frequency (25 [MB/sec] = 25000000 [Byte/sec] at 50 MHz) and data size is based on memory boundary (power of 2).

9.1. Send Interface Condition Command (CMD8)

CMD8 (Send Interface Condition Command) is defined to initialize microSD Memory Cards compliant to the Physical Specification Version 2.00. CMD8 is valid when the card is in Idle state. This command has two Functions:

- Voltage check: Checks whether the card can operate on the host supply voltage.
- Command Enable: Enables expansion of existing command and response. Receiving CMD8 enables new functionality to existing commands by redefining previously reserved bits. ACMD41 is to support initialization of High Capacity microSD Memory Cards.

Table 2: Bit Description

Description	Value (hex)	Width	Bit Position
Start Bit	'0'	1	47
Transmission Bit	'1'	1	46
Command Index	'001000'	6	[45:40]
Reserved Bits	'00000h'	20	[39:20]
Voltage Supplied (VHS)	x	4	[19:16]
Check Patterns	x	8	[15:8]
CRC7	x	7	[7:1]
End Bit	'1'	1	0

Table 3: Voltage

Voltage Supplied(bin)	Value Definition
0000	Not Defined
0001	2.7V-3.6V
0010	Reserved for Low Voltage Range
0100	Reserved
1000	Reserved

When the card is in an idle state, the host shall issue CMD8 before ACMD41. In the argument, 'voltage supplied' is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern. The card checks whether it can operate on the host's supply voltage. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument. If the card does not support the host supply voltage, it shall not return response and stays in Idle state. Table 4 shows the card operation for CMD8.

Table 4: Card Operation

Command Argument Check					Response of Card[5]					
Index	**Reserved**	**VHS**	**Pattern**	**CRC**	**Index**	**Ver**	**Reserved**	**VHS**	**Pattern**	**CRC**
Don't Care	Don't Care	Don't Care	Don't Care	Error	No Response (CRC Error Indication i the following command)					
Not 8	Don't Care	Don't Care	Don't Care	Correct	Depends on command index					
=8	Don't Care	Mismatch[6]	Don't Care	Correct	No Response					
=8	Don't Care	Match[6]	Don't Care	Correct	8	Ver=0	0	Echo Back	Echo Back	Calculate

9.2. Command Functional Difference in High Capacity microSD Memory Card

Memory access commands include block read commands (CMD17, CMD18), block write commands (CMD24, CMD25), and block erase commands (CMD32, CMD33). Following are the functional differences of memory access commands between Standard Capacity and High Capacity microSD Memory Cards:

9.2.1. Command Argument

In High Capacity Cards, the 32-bit argument of memory access commands uses the memory address in block address format. Block length is fixed to 512 bytes, In Standard Capacity Cards, the 32-bit argument of memory access commands uses the memory address in byte address format. Block length is determined by CMD16, i.e.:

- Argument 0001h is byte address 0001h in the Standard Capacity Card and 0001h block in High Capacity Card
- Argument 0200h is byte address 0200h in the Standard Capacity Card and 0200h block in High Capacity Card

9.2.2. Partial Access and Misalign Access

Partial access and Misalign access (crossing physical block boundary) are disabled in High Capacity Card as the block address is used. Access is only granted based on block addressing.

9.2.3. Set Block Length

When memory read and write commands are used in block address mode, 512-byte fixed block length is used regardless of the block length set by CMD16. The setting of the block length does not affect the memory access commands. CMD42 is not classified as a memory access command. The data block size shall be specified by CMD16 and the block length can be set up to 512 bytes. Setting block length larger than 512 bytes sets the BLOCK_LEN_ERROR error bit regardless of the card capacity.

9.2.4. Write Protected Group

High Capacity microSD Memory Card does not support write-protected groups. Issuing CMD28, CMD29 and CMD30 generates the ILLEGAL_COMMAND error.

[5] Response indicates the actual response the card returns. It does not include errors during response transfer.

[6] Match means logical AND of the following conditions: (1) Only one bit is set to 1 in VHS. (2) The card supports the host supply voltage. (3) Mismatch in other cases.

10. Life Monitoring

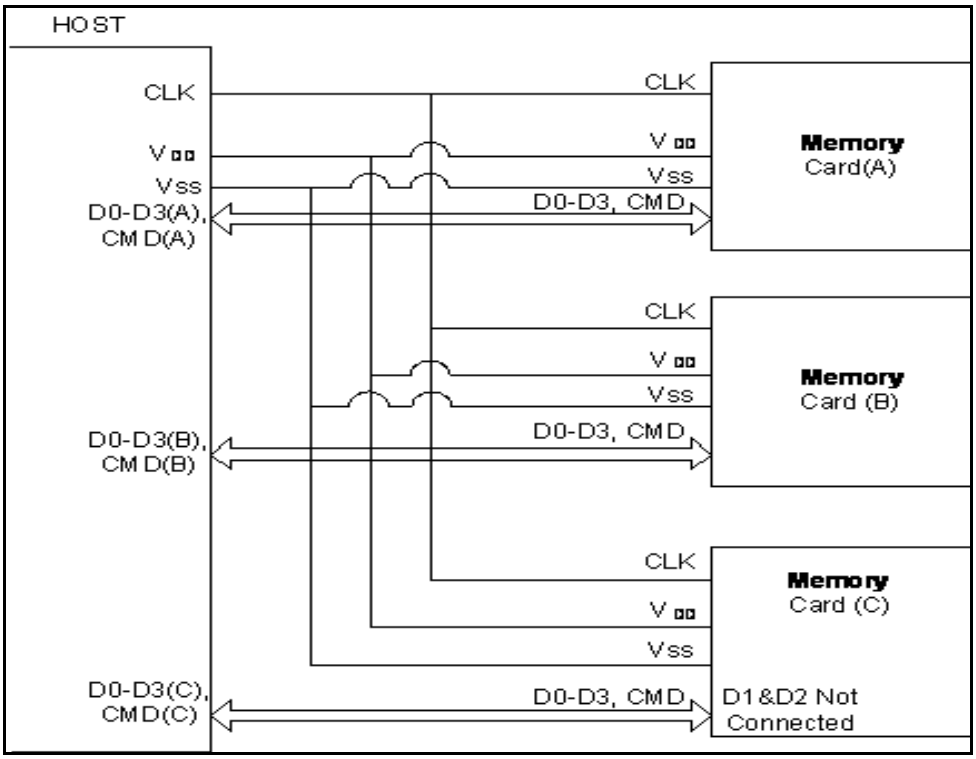
For cards based on Hyperstone and Phison controllers (character 12, Flash Controller = 1, 2, and A), the remaining life of the card is available unders Windows XP/Vista/7 and/or command line interface. Additional SMART commands are supported via command line interface.

11. Function Description

The microSD Card system defines two alternative communication protocols: microSD and SPI. Applications can choose one of these two modes. Mode selection is transparent to the host. The card automatically detects the mode of the command and expects the rest of the communication to be in the same communication mode.

11.1. microSD Bus

Figure 3: microSD Memory Card System Bus System



The microSD bus includes the following signals:

- DAT0 – DAT3: four Bi-directional data signals
- CLK: Host-to-card clock signal
- CMD: Bi-directional Command/Response signals
- VDD, VSS1, VSS2: Power and ground signals

The microSD Memory Card has a master (application), multiple slaves (cards), synchronous star topology (refer to Figure 2). Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0 – DAT3) signals are dedicated to each card providing continues point-to-point connection to all cards.

During the initialization process, commands are sent to each card individually, allowing the application to detect the cards and assign logical address to the physical slots. Data is always sent (received) to (form) each card individually. However, in order to simplify the handling of the card stack, after the initialization process, all

commands may be sent concurrently to all cards. Addressing a card's information is provided in the command packet.

The microSD bus allows dynamic configuration of the data lines. After power up, by default, the microSD Memory Card will use only DAT0 for data transfer. After initialization, the host can change the bus width (number of active data lines). This feature allows easy trade-off between hardware cost and system performance.

Note that while DAT1-DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode).

11.2. SPI Bus

The SPI communication mode of the microSD Card is designed to communicate with SPI channel, commonly found in various micro-controllers. The interface is selected during the first reset command after power up and cannot be changed as long as the part is powered on.

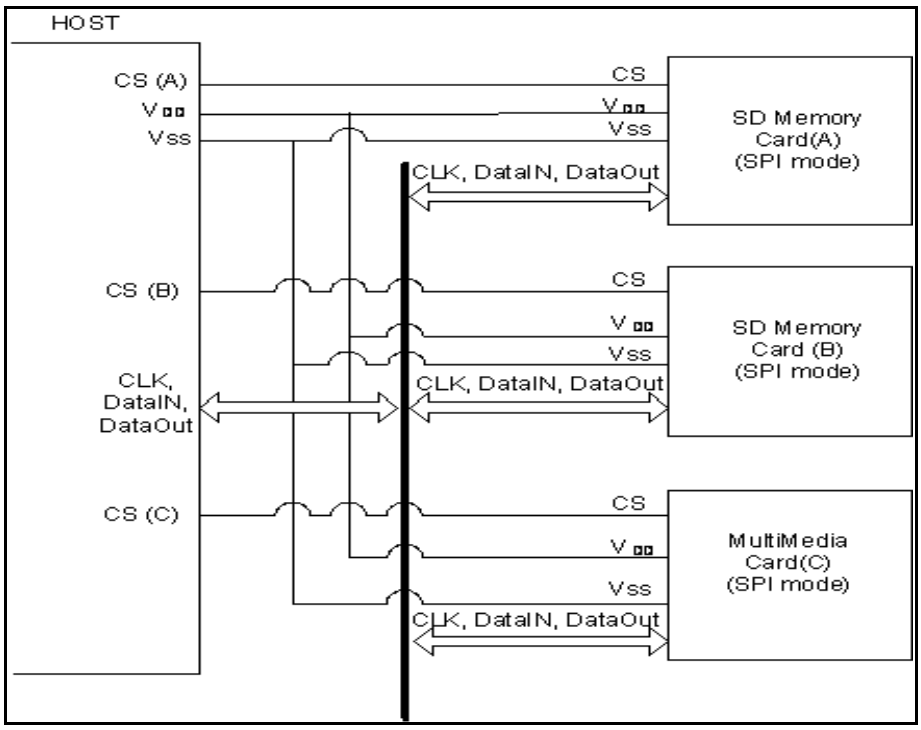
The SPI standard defines the physical link only, and not the complete data transfer protocol. The microSD Memory Card SPI implementation uses the same command set of the microSD mode. From the application point of view, the advantage of the SPI mode is the capability of using an off-the-shelf host, reducing the design effort. The disadvantage is reduction in performance, compare to the microSD mode, which enables the wide bus option.

microSD Memory Card SPI channel consists of the following four signals.

- **CLK**: Host-to-card clock signal.
- **CS**: Host-to-card chip select signal.
- **Data In**: Host-to-card data signal.
- **Data Out**: Card-to-host data signal.

Another SPI common characteristic is byte length data transfer, which is implemented in the card as well. All data tokens are multiples of a byte (8 bit) and always aligned to the CS signal.

Figure 4: microSD Memory Card System (SPI mode) Bus System



The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal (see Figure 4). The SPI interface uses seven signals out of nine uSD signals (DAT1 and DAT2 are not used), DAT3 is the CS signal.

12. Read and Write Operation

12.1. microSD Bus Protocol

12.1.1. Command

A command is a token that starts an operation. A command is sent from the host, either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.

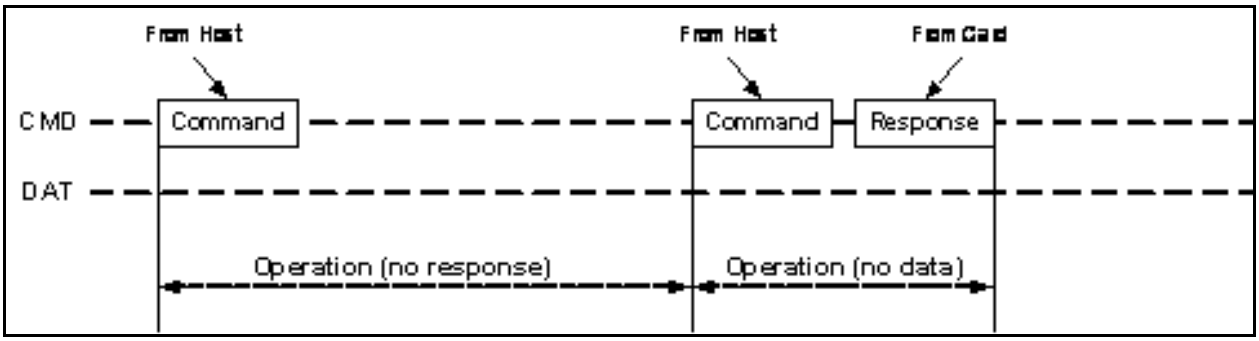
12.1.2. Response

A response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

12.1.3. Data

Data can be transferred from the card to the host or vice versa. Data is transferred via the data line.

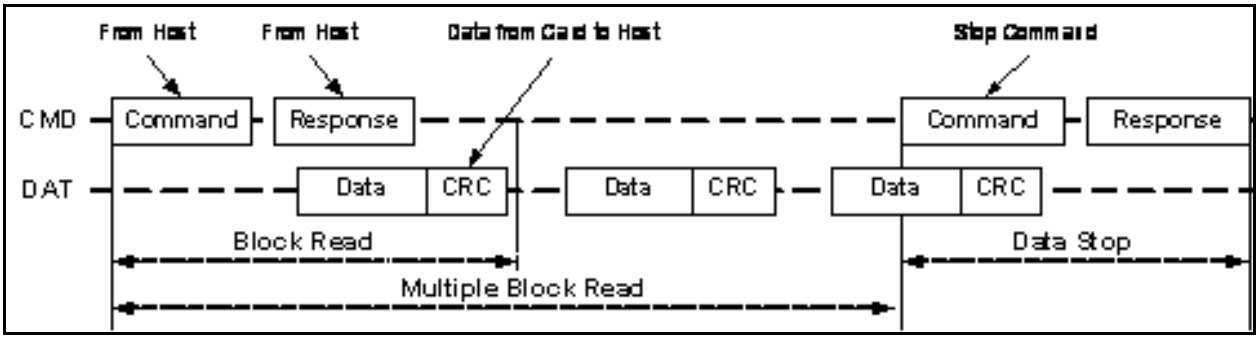
Figure 5: "no response" and "no data" Operations



The basic transaction transfers information directly within the command or response structure. In addition, some operations have a data token.

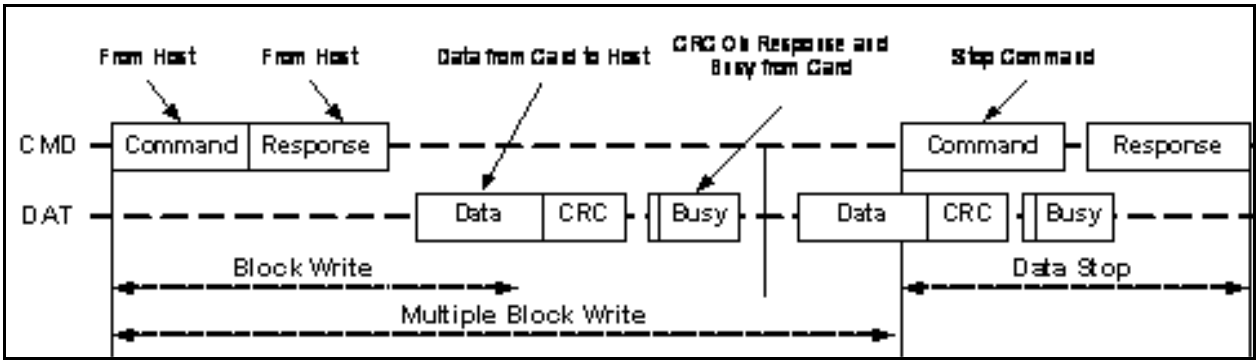
Data transfer to/form the microSD Memory Card are done in blocks always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode provides faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

Figure 6: Multiple Block Read



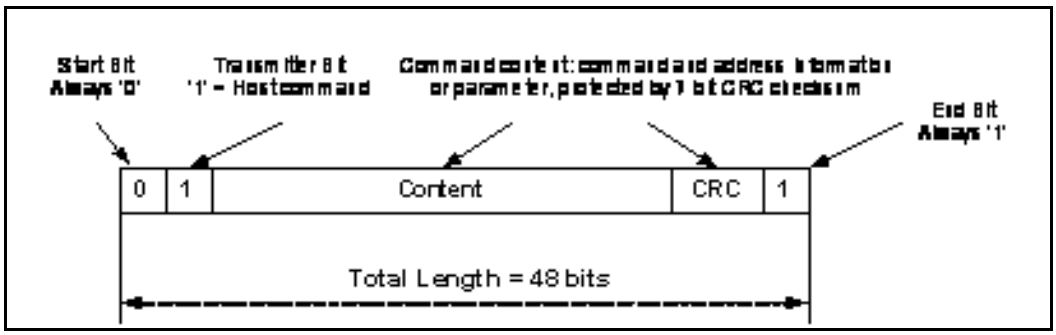
The block write operation uses a simple 'busy signaling' on the DAT0 data line during the write operation, regardless of the number of data lines used for transferring the data.

Figure 7: Multiple Block Write Operation



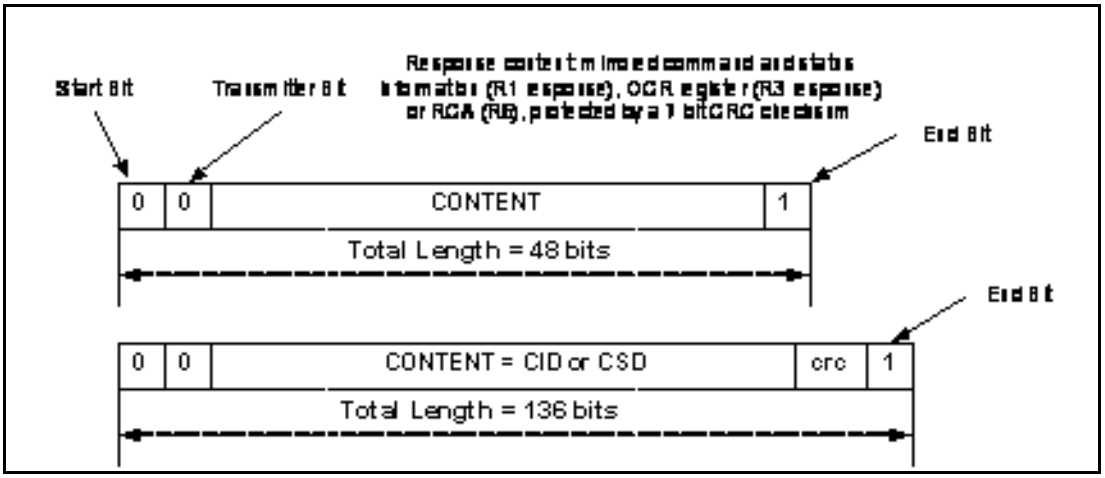
Each Command token is preceded by a start bit and succeeded by an end bit. The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and operation may be repeated.

Figure 8: Command token Format



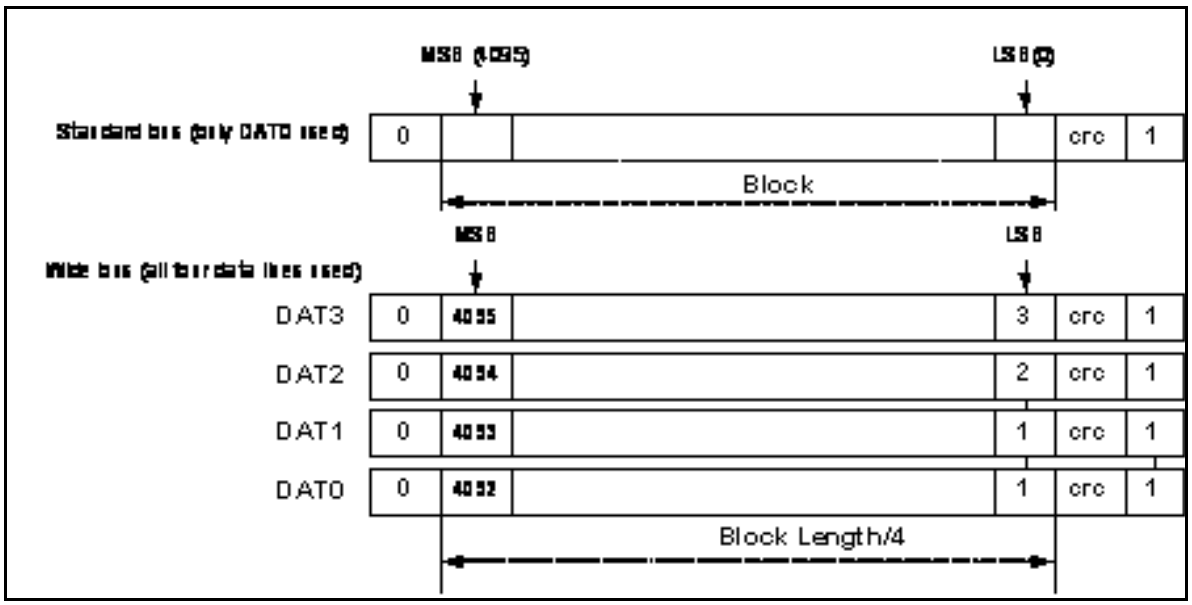
Response tokens have four coding schemes depending on their content. The token length is either 48 or 136 bits.

Figure 9: Response token Format



In the CMD line, the MSB bit is transmitted first, and the LSB bit is the last. When the wide bus option is used, the data is transferred 4-bits at a time (refer to Figure 9). It starts when the end bits and the CRC bits, are transmitted for every DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and busy indication will be sent from the card to the host only on DAT0 (DAT1-DAT3 during that period are 'Don't Care').

Figure 10: Data Packet Format



12.2. SPI Bus Protocol

While the microSD channel is based on command and data bit streams, which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal (i.e. the length is a multiple of 8 clock cycles).

The response behavior in the SPI mode differs from the microSD mode in the following three aspects:

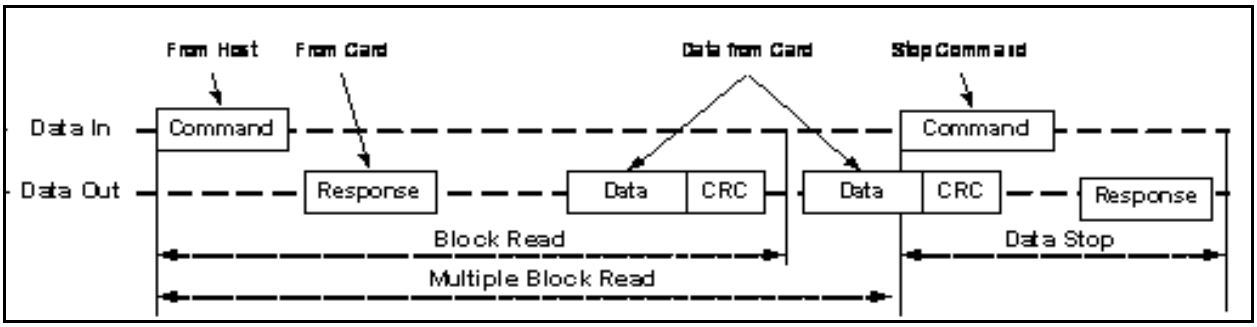
- The selected card always responds to the command.
- Two new response structure is used (8 bits and 16 bits) .
- When the card encounters a data retrieval problem, it will respond with an error response, which replaces the expected data block rather than by a time-out, as in the microSD mode.

In addition to the response command, every data block sent to the card during write operations will be responded with a special data response token.

12.2.1. Data Read

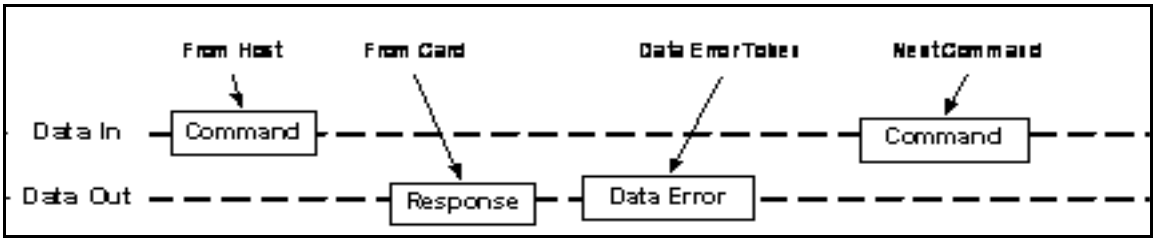
Single and multiple block read commands are supported in SPI mode. However, in order to comply with the SPI industry standard, only two (unidirectional) signals are used. Upon reception of a valid read command, the card will respond with a response token followed by a data token of the length defined in a previous SET_BLOCKEN (CMD16) command. A multiple block read operation is terminated, similar to the microSD protocol, with the STOP_TRANSIMISSION command.

Figure 11: Read Operations



A valid data block is suffixed with a 16 bit CRC generated by the standard CCITT polynomial X16+X12+X5+1. In case of a data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure 12 shows a data read operation that terminated with an error token rather than a data block.

Figure 12: Read Operation - Data Error

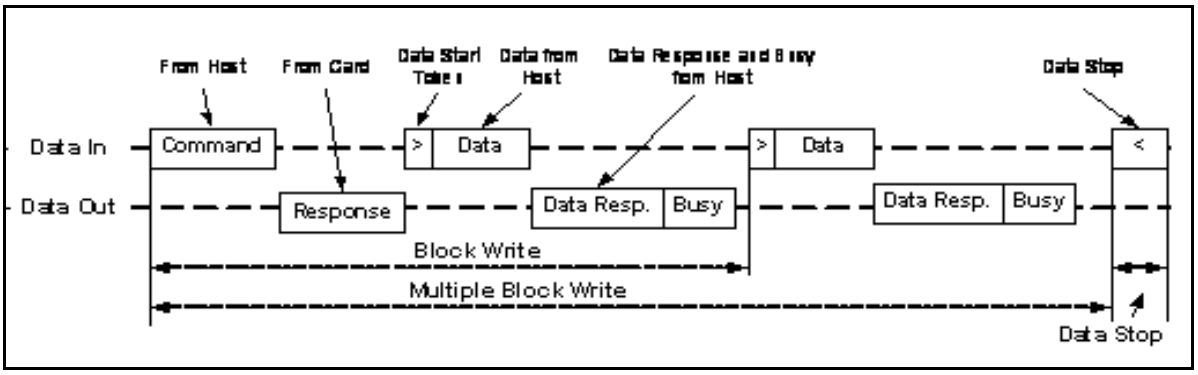


12.2.2. Data Write

Single and multiple block write operations are supported in SPI mode. Upon reception of a valid write command, the card will respond with a response token and will wait for a data block to be sent from the host.

CRC suffix, block length and start address restrictions are identical to the read operation (see Figure 13).

Figure 13: Write Operation



After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the Data Out line low).

13. Card Registers

Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. In order to enable future extensions, the card shall return 0 in the reserved bits of the registers.

13.1. OCR Register

The 32-bit Operation Conditions Register (OCR) stores the voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by the cards.

Bit 7 of OCR is defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets this bit to 1. Additionally, this register includes 2 more status information bits:

- Bit 31 - Card power up status bit: This status bit is set if the card power-up procedure has been completed.
- Bit 30 - Card capacity status bit: This status bit is set to 1 if card is High Capacity microSD Memory Card. A '0' indicates that the card is Standard Capacity microSD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to '1'. The OCR register is implemented by the cards.

Table 5: OCR Register Definitions

OCR Bit Position	OCR Fields Definition
[0-6]	Reserved
[0-6]	Reserved
7	Reserved for Low Voltage Range
[8-14]	Reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
[24 -29]	Reserved
30	Card Capacity Status (CCS)
31	Card Power Up Status Bit (busy)

The supported voltage range is coded as shown in Table 5. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to Low.

13.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (R/W) card has a unique identification number. The structure of the CID register is defined in the following table.

Table 6: CID Register

Name	Field	Width (bits)	Slice	Netlist
Manufacturer ID	MID	8	[127:120]	0110 0001 b
OEM/Application ID	OID	16	[119:104]	4E4C h
Product Name	PNM	40	[103:64]	-
Product Revision	PRV	8	[63:56]	-
Product Serial Number	PSN	32	[55:24]	-
Reserved	-	4	[23:20]	-
Manufacturing Date	MDT	12	[19:8]	-
CRC7 Checksum	CRC	7	[7:1]	-
Not Used, Always 1	-	1	[0:0]	-

MID

MID is a 8-bit binary number that identifies the card manufacturer. The MID number is controlled, defined, and allocated to a microSD Memory Card by the SD-3C, LLC to ensure uniqueness of the CID register.

OID

OID is a 2-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined, and allocated to a microSD Memory Card manufacturer by the SD-3C, LLC to ensure uniqueness of the CID register.

PNM

The product name (PNM) is a 5-character ASCII string.

PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an “n.m” revision number. The “n” is the most significant nibble and “m” is the least significant nibble. As an example, the PRV binary value field for product revision “6.2” will be: 0110 0010b.

13.3. CSD Register

The Card-Specific Data register provides information regarding access to the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27.

13.4. CSD Register (CSD Version 2.0)

CSD Version 2.0 is applied to only the High Capacity microSD Memory Card. The field names in parenthesis in the below CSR table are set to fixed values and indicate that the host is not required for addressing these fields. These fixed values enable host, to keep compatibility to CSD Version 1.0.

The Cell Type field is coded as follows: R = read-only, W(1) = write once, W = multiple write.

Table 7: CSD Register Fields version 2.0

Name	Field	Width	Value	Cell Type	CSD-slice
CSD Structure	CSD_STRUCTURE	2	01b	R	[127:126]
Reserved	-	6	000000b	R	[125:120]
Data Read Access-time	(TAAC)	8	0Eh	R	[119:112]
Data Read Access-time In CLK Cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
Max. Data Transfer Rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
Card Command Classes	CCC	12	01x11011010b	R	[95:84]
Max. Read Data Block Length	(READ_BL_LEN)	4	9h	R	[83:80]
Partial Blocks For Read Allowed	(READ_BL_PARTIAL)	1	0b	R	[79:79]
Write Block Misalignment	(WRITE_BLK_MISALIGN)	1	0b	R	[78:78]
Read Block Misalignment	(READ_BLK_MISALIGN)	1	0b	R	[77:77]
DSR Implemented	DSR_IMP	1	xb	R	[76:76]
Reserved	-	6	000000b	R	[75:70]
Device Size	C SIZE	22	00xxxxh	R	[69:48]
Reserved	-	1	0b	R	[47:47]
Erase Single Block Enable	(ERASE_BLK_EN)	1	1b	R	[46:46]
Erase Sector Size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
Write Protect Group Size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
Write Protect Group Enable	(WP_GRP_ENABLE)	1	0b	R	[31:31]
Reserved	-	2	00b	R	[30:29]
Write Speed Factor	(R2W_FACTOR)	3	010b	R	[28:26]
Max. Write Data Block Length	(WRITE_BL_LEN)	4	9h	R	[25:22]
Partial Blocks For Write Allowed	(WRITE_GRP_ENABLE)	1	0b	R	[21:21]
Reserved	-	5	00000b	R	[20:16]
File Format Group	(FILE_FORMAT_GRP)	1	0b	R	[15:15]
Copy Flag (OTP)	COPY	1	xb	R/W(1)	[14:14]
Permanent Write Protection	PERM_WRITE_PROJECT	1	xb	R/W(1)	[13:13]
Temporary Write Protection	TWP_WRITE_PROTECT	1	xb	R/W	[12:12]
File Format	(FILE_FORMAT)	2	00b	R	[11:10]
Reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
Not Used, Always '1'	-	1	1b	-	[0:0]

Table 8: CSD Register Field Definitions

CSD_STRUCTURE	Field structures of the CSD register depends on the Physical Specification Version and Card's Capacity. The CSD_STRUCTURE field in the CSD register indicates it's structure version.
TAAC	This field is fixed to 0Eh, which indicates 1 ms and it indiccates the host should not use TAAC, NSAC, and R2W_FACTOR to calculate time out. It should uses fixed time out values for read and write operations.
NSAC	This field is fixed to 00h. NSAC should not be used to calculate time-out values.
TRAN_SPEED	Definition of this field is same as in CSD Version1.0.
CCC	Definition of this field is same as in CSD Version1.0.
READ_BL_LEN	This field is fixed to 9h, which indicates READ_BL_LEN=512 Bytes.
READ_BL_PARTIAL	This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.
WRITE _BLK_MISALIGN	This field is fixed to 0, which indicates write access crossing physical block boundaries is always disabled in High Capacity microSD Memory Card.
READ_BLK_MISALIGN	This field is fixed to 0, which indicates read access crossing physical block boundaries is always disabled in High Capacity microSD Memory Card.
DSR_IMP	Definition of this field is same as in CSD Version1.0.
C_SIZE	This field is expanded to 22 bits and can indicate up to 2 T Bytes (It is the same as the maximum memory space specified by a 32-bit block address.) This parameter is used to calculate the user data area capacity in the microSD memory card (not included the protected area). The user data area capacity is calculated from C_SIZE as follows Memory capacity = (C_SIZE+1) * 512K byte. As the maximum capacity of the Physical Layer Specification Version 2.00 is 32 GB, the upper 6 bits of this field shall be set to 0.
ERASE_BLK_EN	This field is fixed to 1, which means the host can erase one or multiple units of 512 bytes.
SECTOR_SIZE	This field is fixed to 7Fh, which indicates 64 K Bytes. This value does not relate to erase operation. Version 2.00 cards indicates memory boundary by AU size and this field should not be used.
WP_GRP_SIZE	This field is fixed to 00h. The High Capacity microSD Memory Card does not support write protected groups.
WP_GRP_ENABLE	This field is fixed to 0. The High Capacity microSD Memory Card does not support write protected groups.
R2W_FACTOR	This field is fixed to 2h, which indicates 4 multiples. Write time out can be calculated by multiplying the read access time and R2W_FACTOR. However, the host should not use this factor and should use 250 ms for write time out
WRITE_BL_LEN	This field is fixed to 9h, which indicates WRITE_BL_LEN=512 Byte.
WRITE_BL_PARTIAL	This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.
FILE_FORMAT_GRP	This field is set to 0. Host should not use this field.
COPY	Definition of this field is same as in CSD Version1.0.
PERM_WRITE_PROTECT	Definition of this field is same as in CSD Version1.0.
TMP_WRITE_PROTECT	Definition of this field is same as in CSD Version1.0.
FILE_FORMAT	This field is set to 0. Host should not use this field.
CRC	Definition of this field is same as in CSD Version1.0.

13.5. RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000, which is reserved to set all cards into the Stand-by State with CMD7.

13.6. DSR Register (Optional)

The 16-bit Driver Stage Register can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate, or number of cards). The CSD register carries information about DSR register usage. The default value of the DSR register is 0x404.

13.7. SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the microSD Memory Card's special features that can be configured into a card. The size of SCR register is 64 bits. This register is set in the factory by the microSD Memory Card manufacturer.

The following table describes the SCR register content.

Table 9: SCR fields

Description	Field	Width	Cell Type	SCCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
microSD Memory Card, Spec, Version	SD_SPEC	4	R	[59:56]
Data staus after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
microSD Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
Reserved	-	16	R	[47:32]
Reserved for manufacturer	-	32	R	[31:0]

Table 10: SCR Register Structure Version

SCR STRUCTURE	SCR Structure Version	microSD Physical Layer Specification Version
0	SCR Version No. 1.0	Version 1.01-2.00
[1-15]	Reserved	

13.7.1. SD_SPEC

Describes the Physical Layer Specification Versions supported by the card.

Table 11: Physical Layer Specification Version

SD_SPEC	Physical Layer Specification Version Number
0	Version 1.0-1.01
1	Version 1.10
2	Version 2.00
[3-15]	Reserved

13.7.2. DATA_STAT_AFTER_ERASE

DATA_STAT_AFTER_ERASE defines the data status after erase, whether it is 0 or 1 (the status is card vendor dependent).

13.7.3. SD_SECURITY

Describes the Security Specification Version supported by the card.

Table 12: microSD Supported Security Algorithm[7]

SD_ SECURITY	Security Specification Version
0	No Security
1	Not Used
2	Version 1.01
3	Version 2.00
[4-7]	Reserved

13.7.4. SD_BUS_WIDTHS

Describes all the DAT bus widths that are supported by this card.

Table 13: Supported Bus Widths

SD_BUS_WIDTHS	Supported Bus Widths
Bit 0	1 bit (DAT0)
Bit 1	Reserved
Bit 2	4 bit/DAT[0-3]
Bit 3	Reserved

Since the microSD Memory Card supports at least the two bus mode width, 1-bit or 4-bit width, any microSD Card should set at least bits 0 and 2 (SD_BUS_WIDTH=”0101”).

[7] It is mandatory for a regular writable microSD Memory Card to support Security Protocol. For ROM (Read Only) and OTP (One Time Programmable) types of the microSD Memory Card, the security feature is optional. In the case of Standard Capacity microSD Memory Card, this field shall be set to 2 (Version 1.01). In the case of High Capacity microSD Memory Card, this field shall be set to 3 (Version 2.00).

14. Product Specifications

14.1. External Signal Contacts (ESC)

Table 14: Package – External Signal Contacts

Number of ESC	8 minimum
Distance From Front Edge	1.1mm
ESC Grid	1.1mm
Contact Dimensions	0.8mm x 2.9mm
Electrical Resistance	30 mOhm (worst case: 100 mOhm)

14.2. Design and Format

Table 15: microSD Memory Card Package Dimensions

Dimensions: **microSD package**	11 mm x 15 mm; (min. 10.9mm x 14.9mm; max.11.1mm x 15.1 mm) (Testing according to MIL STD 883, Method 2016)
Thickness	Inter Connect Area: 0.7mm+/-0.05mm, see Fig. 14 (C1) Card Thickness: 0.95mm Max see Fig 14 (C1 + C3) Pull Area: 1.0mm +/-0.1mm see Fig 14 (C)
Printable area	Suggested Outside Keep out Area
Surface	Plain (except contact area)
Edges	Smooth edges
Inverse insertion	Protection on right corner (top view)
Position of ESC contacts	Along middle of shorter edge

14.3. Reliability and Durability

Table 16: Reliability and Durability

Operating Temperature	Industrial: -40°C +85°C (with SLC NAND Flash)
Moisture and Corrosion	Operation: 25°C /95% rel.humidity Storage: 40/93% rel.hum./500h Salt water spray: 3% NaCl/35C, 24h ; acc. MIL STD Method 1009
Durability	10,000 mating cycles
Bending[8]	10N
Torque[8]	0.10N*m, ± 2.5° Max
Drop Test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm^2 according to ISO 7816-1
Visual inspection of shape and form[8]	No mold skin; complete form; no cavities Surface smoothness ≤0.1mm/cm^2 within contour; no cracks, No pollution (fat, oil dust, etc.)

[8] SDA's recommended test methods for torque, bending and warpage are defined separately.

14.4. Electrical Static Discharge (ESD) Requirement

Netlist uSD cards can form to the following standards:

ESD testing should be conducted according to IEC 61000-4-2

ESD parameters:

- Human Body Model: ±4 kV 100pF/1.5kΩ
- Machine model: ±0.25 kV 200pF/0Ω

Contact Pads:

±4KV, Human Body Model according to IEC 61000-4-2

Non contact Pads area:

±8kV (coupling plane discharge)

±15kV (air discharge)

Human Body Model according to IEC61000-4-2

15. Mechanical Form Factor

15.1. microSDvault™ Mechanical Dimensions

Figure 14: microSDvault™ Mechanical Description: Top View

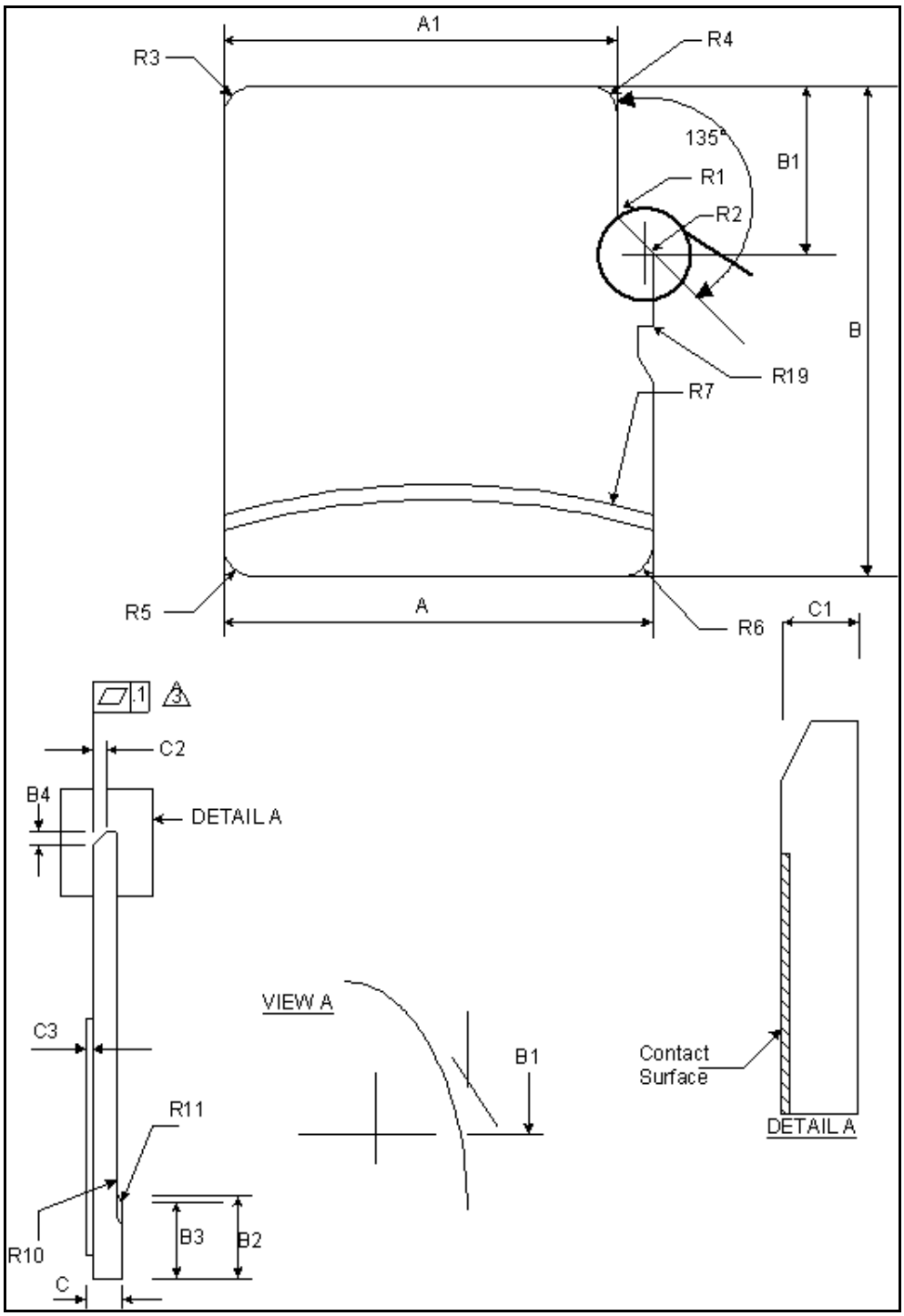


Figure 15: microSDvault™ Mechanical Description (Bottom View)

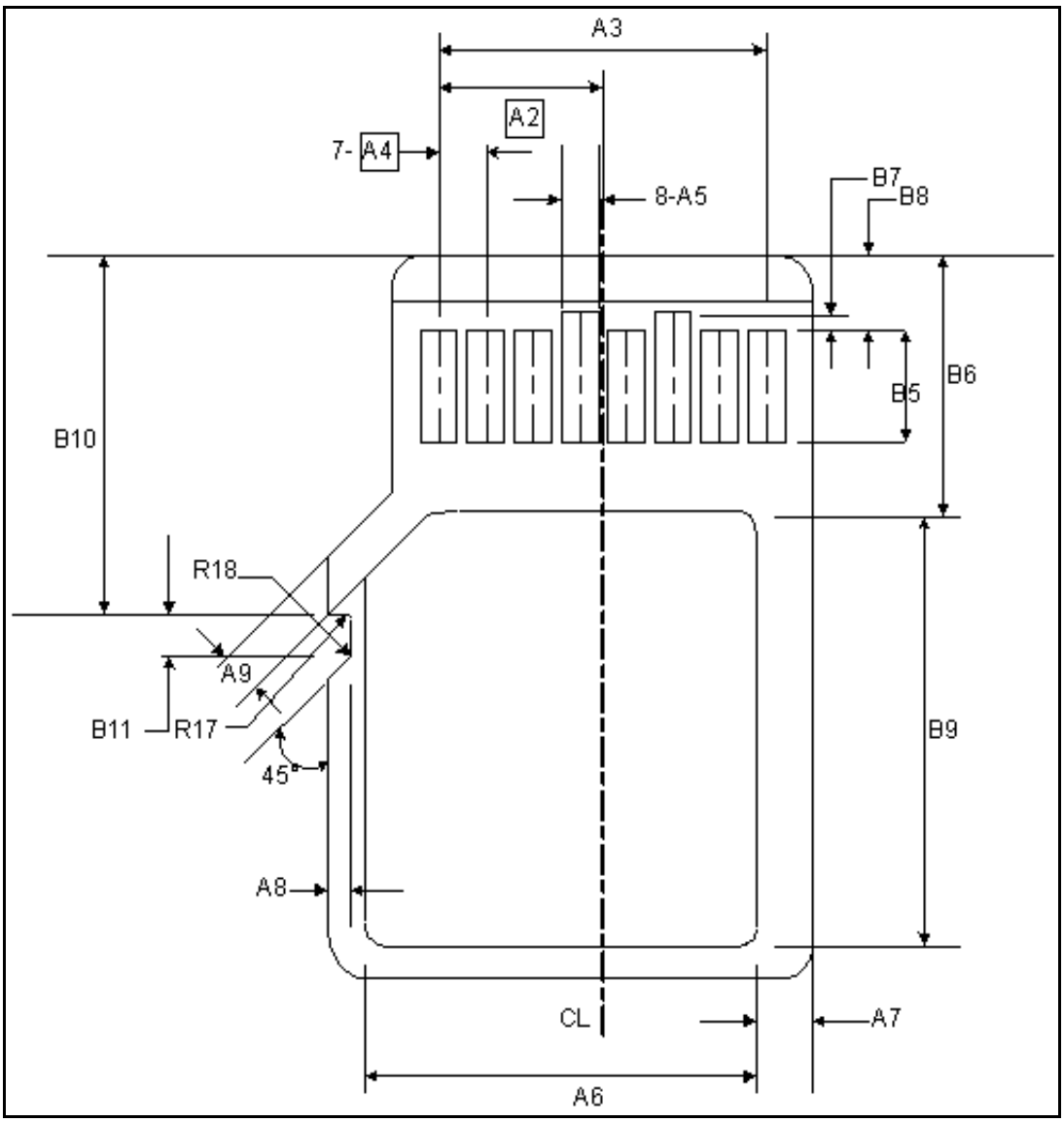


Figure 16: microSDvault™ Mechanical Description (Keep Out Area)

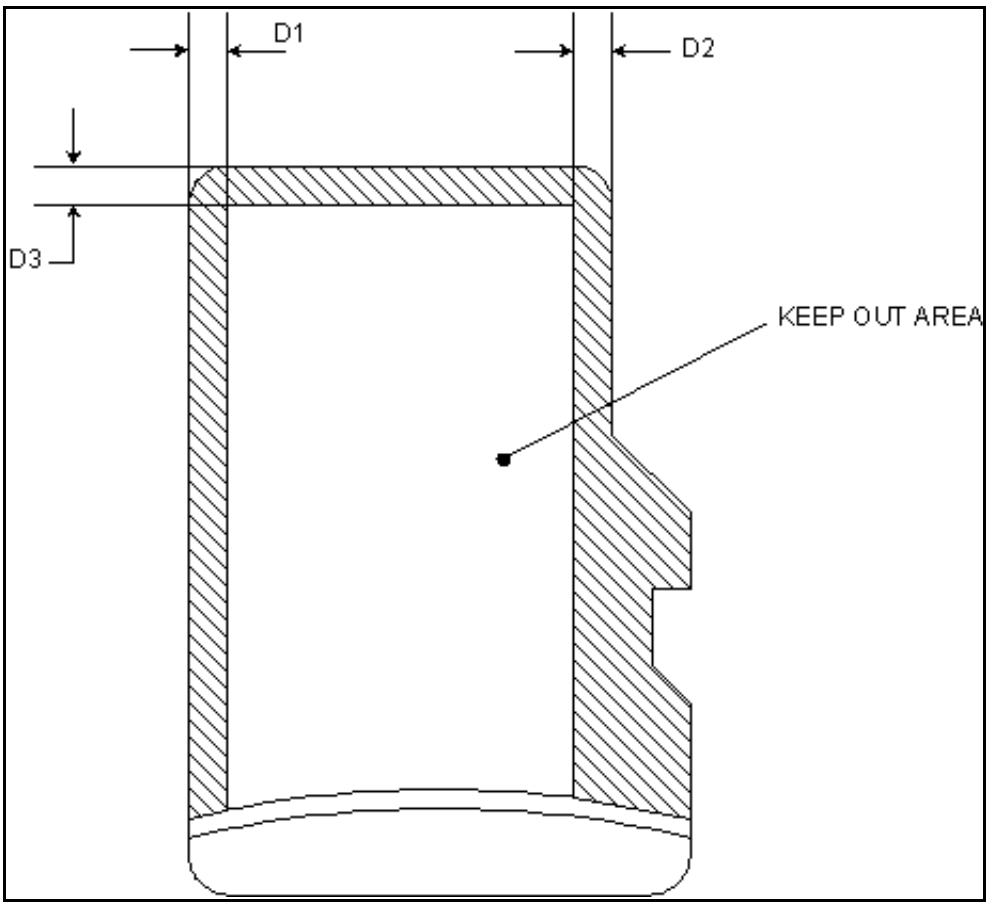


Figure 17: microSDvault™ Memory Card Package – Dimensions[9] [10] [11] [12] [13] [14]

Symbol	Dimensions			Units	Note
	Min	Nom	Max		
A	10.90	11.00	11.10	mm	
A1	9.60	9.70	9.80	mm	Basic
A2	-	3.85	-	mm	
A3	7.60	7.70	7.80	mm	Basic
A4	-	1.10	-	mm	
A5	0.75	0.80	0.85	mm	
A6	-	-	8.50	mm	
A7	0.90	-	-	mm	
A8	0.60	0.70	0.80	mm	
A9	0.80	-	-	mm	
B	14.90	15.00	15.10	mm	
B1	6.30	6.40	6.50	mm	
B2	1.64	1.84	2.40	mm	
B3	1.30	1.50	1.70	mm	
B4	0.42	0.52	0.62	mm	
B5	2.80	2.90	3.00	mm	
B6	5.50	-	-	mm	
B7	0.20	0.30	0.40	mm	
B8	1.00	1.10	1.20	mm	
B9	-	-	9.00	mm	
B10	7.80	7.90	8.00	mm	
B11	1.10	1.20	1.30	mm	
C	0.90	1.00	1.10	mm	
C1	0.60	0.70	0.80	mm	
C2	0.20	0.30	0.40	mm	
C3	0.00	-	0.15	mm	
D1	1.00	-	-	mm	
D2	1.00	-	-	mm	
D3	1.00	-	-	mm	
R1	0.20	0.40	0.60	mm	
R2	0.20	0.40	0.60	mm	

[9] Dimensioning and Tolerance per ASME Y14.5M-1994.

[10] Coplanarity is additive to C1 Max thickness.

[11] Power supply; I: input; O: output using push – pull drivers; PP: I/O using push – pull drivers

[12] The extended DAT line (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards

[13] After power up this line is input with 50KΩ pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

[14] NC pins should be left open.

Symbol	Dimensions			Units	Note
	Min	Nom	Max		
R3	0.70	0.80	0.90	mm	
R4	0.70	0.80	0.90	mm	
R5	0.70	0.80	0.90	mm	
R6	0.70	0.80	0.90	mm	
R7	29.50	30.00	30.50	mm	
R10	-	0.20	-	mm	
R11	-	0.20	-	mm	

16. DC Characteristics

Following tables define all D.C. characteristics for the microSD card.

Table 17: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Operating Temperature Range	T_{AMB}	-40°C to +85°C
Storage Temperature	$T_{STORAGE}$	-40°C to +125°C
Voltage on any pin with respect to GND.	V_{MAX}	-0.3V min. to V_{DD} + 0.3V max.

Table 18: Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Vcc Voltage	Vcc	3.0	3.3	3.6	V
Read Current	Ir	10	15	20	mA
Write Current	Iw	20	25	30	mA
Idle Current	Ii	100	115	130	uA
Operating Temperature	Ta	-40		85	°C

Table 19: Bus Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.7	3.6	V	
V_{DD}	microSD Low Voltage Supply	1.6	3.6	V	
V_{IL}	Input LOW Voltage	V_{SS}-0.3	0.25*V_{DD}	V	
V_{IH}	Input HIGH Voltage	0.625* V_{DD}	V_{DD}+ 0.3	V	
V_{OL}	Output LOW Voltage		0.125* V_{DD}	V	at 100µA
V_{OH}	Output HIGH Voltage	0.75* V_{DD}		V	at 100µA

Table 20: Leakage Current

Symbol	Parameter	MIN	MAX	Units
I_{LI}	Input Leakage Current	-10	+10	µA
I_{LO}	Output Leakage Current	-10	+10	µA

17. AC Characteristics

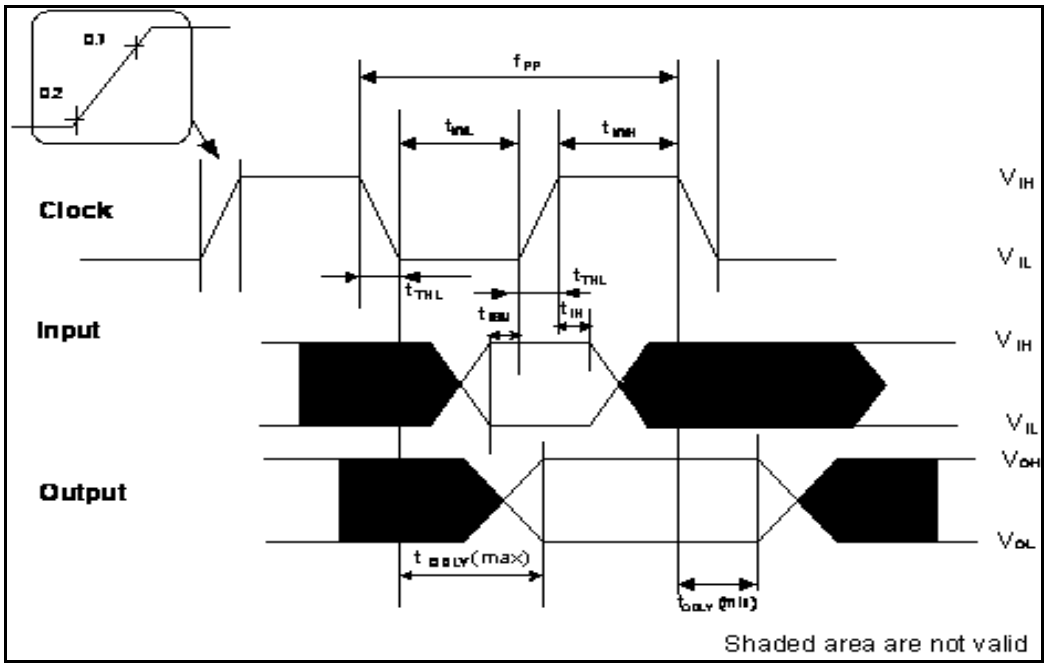
The microSD card interface characteristics refer to the symbols used in the timing definition of the microSD 2.0 standards.

17.1. microSD Card Timing Specification (Low Speed mode)

Table 21: Timing Specification (Low Speed mode)

Symbol	Item	MIN	MAX	Units	Notes
f_{PP}	Clock, Data transfer mode	0	25	MHz	$C_{CARD} \leq 10pF$
f_{OD}	Clock, Identification mode	0	400	kHz	$C_{CARD} \leq 10pF$
t_{WL}	Clock Low Time	10		ns	$C_{CARD} \leq 10pF$
t_{WH}	Clock High Time	10		ns	$C_{CARD} \leq 10pF$
t_{TLH}	Clock Rise Time		10	ns	$C_{CARD} \leq 10pF$
t_{THL}	Clock Fall Time		10	ns	$C_{CARD} \leq 10pF$
t_{ISU}	CMD, DAT input setup time	5		ns	$C_{CARD} \leq 10pF$
T_{IH}	CMD, DAT input hold time	5		ns	$C_{CARD} \leq 10pF$
t_{ODLY}	CMD, DAT output delay time during Data Transfer Mode	0	14	ns	$C_{CARD} \leq 40pF$
t_{ODLY}	CMD, DAT output delay time during Identification Mode	0	50	ns	$C_{CARD} \leq 40pF$

Figure 18: Timing Diagram (Low Speed Mode)

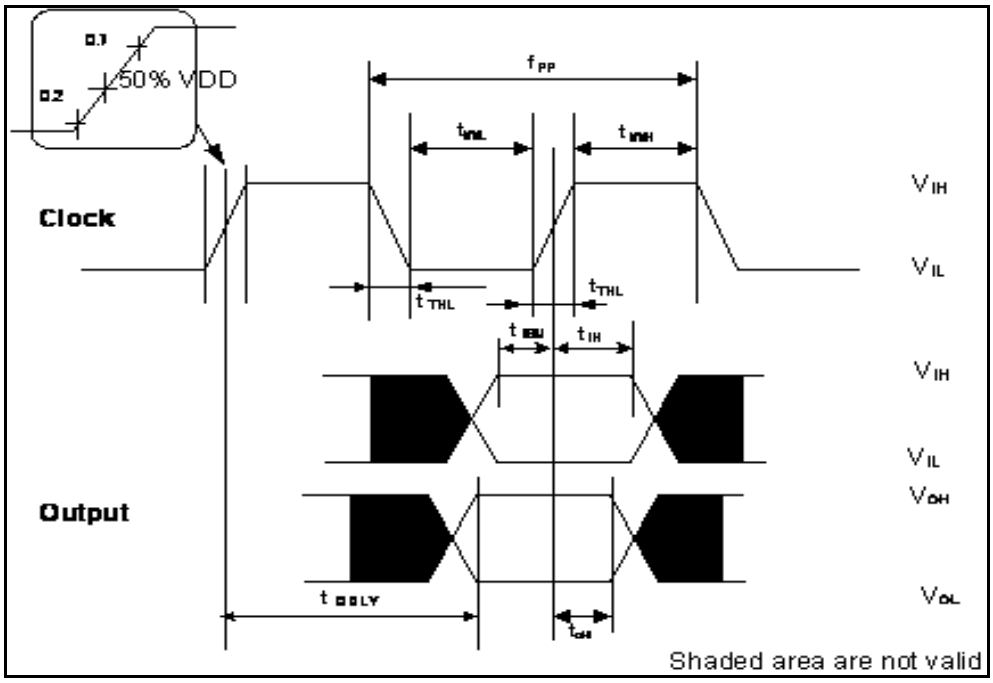


17.2. microSD Card Timing Specification (High Speed mode)

Table 22: Timing Specification (High Speed mode)

Symbol	Item	MIN	MAX	Units	Notes
f_{PP}	Clock, Data transfer mode	0	50	MHz	C_{CARD} ≤ 10pF
t_{WL}	Clock Low Time	7		ns	C_{CARD} ≤ 10pF
t_{WH}	Clock High Time	7		ns	C_{CARD} ≤ 10pF
t_{TLH}	Clock Rise Time		3	ns	C_{CARD} ≤ 10pF
t_{THL}	Clock Fall Time		3	ns	C_{CARD} ≤ 10pF
t_{ISU}	CMD, DAT input setup time	6		ns	C_{CARD} ≤ 10pF
T_{IH}	CMD, DAT input hold time	2		ns	C_{CARD} ≤ 10pF
t_{ODLY}	CMD, DAT output delay time during Data Transfer Mode	0	14	ns	C_{CARD} ≤ 40pF
t_{ODLY}	CMD, DAT output delay time during Identification Mode	0	50	ns	C_{CARD} ≤ 40pF
t_{OH}	Output Hold time	2.5		ns	C_{CARD} ≤ 40pF
C_L	System Capacitance		40	pF	1 Card

Figure 19: Timing Diagram (High Speed Mode)



18. Revision History

Revision	Date	Author	Notes
1v0	March 12, 2014	--	Initial Release
1v1	June 2, 2010	--	Corrected part numbering schema
1v2	July 20, 2010	--	Updated part numbering schema
1v3	October 27, 2010	--	Updated formatting and content
1v4	April 20, 2011	HS	Corrected Part number information in header block; Promoted document to Data sheet from Preliminary Data sheet; Corrected Industrial Temperature range; Added power numbers; Added Class 10
1v5	May 2, 2011	HS	Added DC and AC characteristics
1v6	April 4, 2012	HS	Changed the part numbers to new part number format Added new part number decoder to the datasheet
1v7	October 14, 2013	DP	Updated part numbering schema and decoder
1v8	March 20, 2014	BR	Updated decoder

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