NETLIST

Datasheet

**CFvault™ II - Compact Flash**

**128MB to 16GB**

**NLCF*abc*UA*d*-3*v*SHAA*wxyz*0**

## 1. Overview

Netlist, the pioneer in the development of high-density memory subsystems, is proud to offer the Netlist CFvault™ II CompactFlash Storage Card, which provides 128MB to 16GB of nonvolatile storage. The Netlist solution uses a controller that provides a fully compatible PCMCIA interface to the Flash memory. Netlist's CFvault™ II Storage card is the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature. Because there are no moving parts to service or maintain, CF Storage card is a reliable alternative to a mechanical hard disk drive for high availability and mission critical applications. While the inherent ruggedness and reliability of solid-state storage relative to rotating hard drives is intuitive, new OEM applications are emerging due to the low cost per usable megabyte. Most applications that use embedded operating systems such as VxWorks™, Windows XP/embedded™, and Linux™ do not have large data storage requirements, and therefore a cost savings can be realized when using this robust media.

The Netlist CFvault™ II CompactFlash (CF) Storage Card provides a Write-Protect function that prevents the card from being written, modified and deleted. The Netlist CFvault™ II CompactFlash (CF) Storage Card also provides high capacity data storage that electrically complies with the Personal Computer Memory Card International Association (PCMCIA) standard. The Netlist CFvault™ II CF Storage Card also can sense your system's requirements and operate in True IDE Mode that is electrically compatible with an IDE disk drive. The on-card intelligent controller manages interface protocols, data storage and retrieval as well as Error Correcting Code (ECC), detects handling and diagnostics, power management and clock control.

## 2. System Features

- 128MB to 16GB of mass storage data utilizing SLC and MLC flash technology
- Non-volatile storage and completely solid state (No Moving Parts)
- Fully compliant to CFA 3.0, and PCMCIA 2.1 specifications
- Supports PIO mode 6, MDMA mode 4 and UDMA mode 4 (in True-IDE)
- Fixed and removable configurations available
- PC Card ATA and True IDE mode compatible
- Form factor: CF Type I
- Dual channel with two direct flash memory access (DFA) units
- Advanced wear leveling algorithm
- Card Information Structure (CIS) Programmed into 256 Bytes of Internal Memory
- Bad block management
- Sudden power-fail management
- 5V or 3.3V power supply
- RS-ECC engine with 4 symbol correction
- RoHS-6 compliant (Pb-free)
- Write-Protect switch
- Industrial and Commercial temperature



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# 3. ORDERING INFORMATION

Ultra DMA Mode 4 in True IDE Mode & Auto Detect

| **Part Number: 128MB to 16GB Compact Flash**<br>NLCF*abc*UA*d*-3*v*SHAA*wxyz*0 | | | | | | |
|---|---|---|---|---|---|---|
| abc =<br>Density | d =<br>Temperature Range | v =<br>Flash Manufacturer | w =<br>Flash Die Geometry | x =<br>#CE per Flash Location | y =<br>#Flash Locations | z =<br>#Die per Flash Location |
| 012 = 128MB<br>025 = 256MB<br>051 = 512MB<br>01G = 1GB<br>02G = 2GB<br>04G = 4GB<br>08G = 8GB<br>16G = 16GB | I = Industrial -<br>40°C to +85°C<br>C = Commercial<br>0°C to +70°C | S = Samsung<br>M = Micron<br>T = Toshiba<br>5 = Spansion | 4 = 4xnm<br>3 = 3xnm<br>2 = 2xnm<br>1 = 1xnm | 1 = 1 CE per Flash Location<br>2 = 2 CE per Flash Location<br>4 = 4 CE per Flash Location<br>8 = 8 CE per Flash Location | 1 = 1 Flash Location<br>2 = 2 Flash Locations<br>4 = 4 Flash Locations | 1 = 1 Die per Flash Location<br>2 = 2 Die per Flash Location<br>4 = 4 Die per Flash Location<br>8 = 8 Die per Flash Location |

| **Density** | **Industrial Temperature Part Number** | **Commercial Temperature Part Number** | **Life Cycle Support** |
|---|---|---|---|
| 128MB | NLCF012UAI-35SHAA41110 | NLCF012UAC-35SHAA41110 | 2Q 2019 |
| 256MB | NLCF025UAI-35SHAA41210 | NLCF025UAC-35SHAA41210 | |
| 512MB | NLCF051UAI-35SHAA41210 | NLCF051UAC-35SHAA41210 | |
| 1GB | NLCF01GUAI-35SHAA41210 | NLCF01GUAC-35SHAA41210 | |
| 2GB | NLCF02GUAI-35SHAA42220 | NLCF02GUAC-35SHAA42220 | |
| 4GB | NLCF04GUAI-35SHAA42420 | NLCF04GUAC-35SHAA42420 | |
| 8GB | NLCF08GUAI-3TSHAA32240 | NLCF08GUAC-3TSHAA32240 | 4Q 2015<br>NAND Transition |
| 16GB | NLCF16GUAI-3TSHAA32440 | NLCF16GUAC-3TSHAA32440 | |


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# 4. BLOCK DIAGRAM

**FIGURE 1: NETLIST CFVAULT™ II COMPACT FLASH CONFIGURATION USING SINGLE DIE FLASH DEVICES**

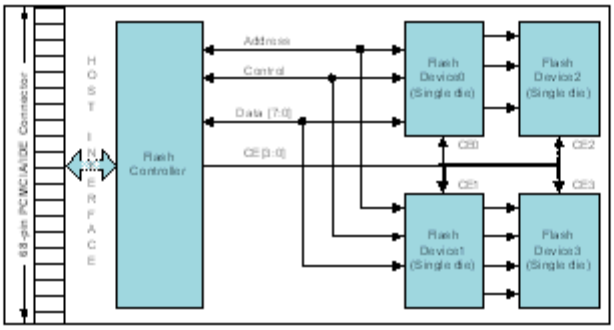



**FIGURE 2: NETLIST CFVAULT™ II COMPACT FLASH CONFIGURATION USING DUAL DIE FLASH DEVICES**

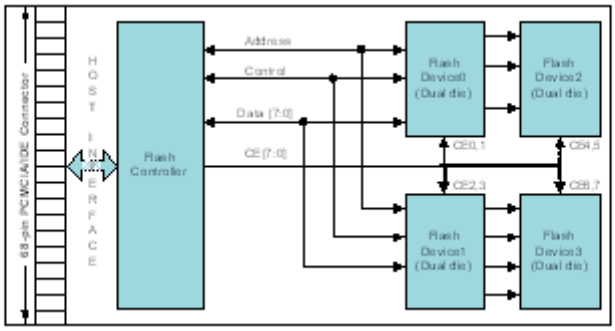
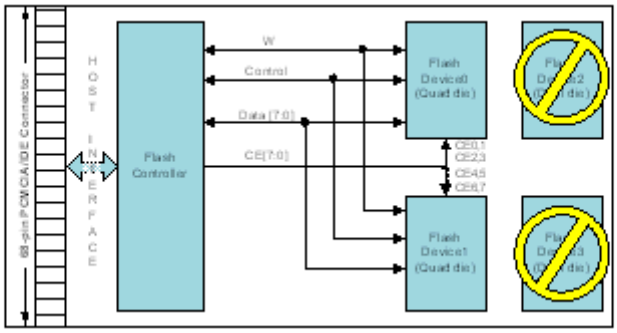



**FIGURE 3: NETLIST CFVAULT™ II COMPACT FLASH CONFIGURATION USING QUAD DIE FLASH DEVICES**





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# 5. PHYSICAL SPECIFICATIONS

## 5.1. CF STORAGE CARD TYPE 1 FORM-FACTOR

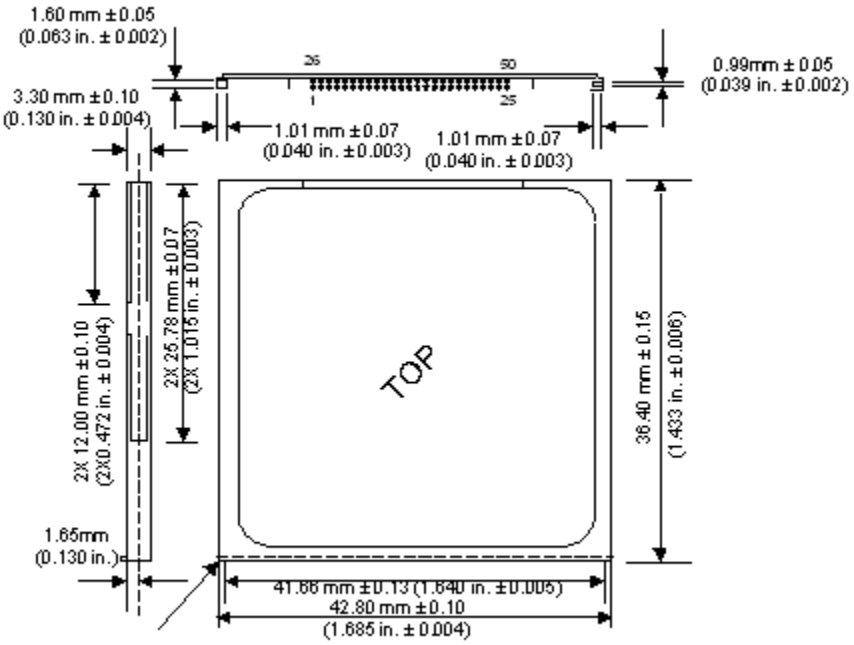
The host is connected to the CF Storage Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

**TABLE 1: CF-CARD FORM FACTOR**

| | |
|---|---|
| **Length** | 36.4 ± 0.15 mm (1.433 ± 0.006 in.) |
| **Width** | 42.80 ± 0.10 mm (1.685 ± 0.004 in.) |
| **Thickness Including Label Area** | 3.3 mm ± 0.10 mm (0.130 ± 0.004 in.) |

## 5.2. PHYSICAL DIAGRAM

**FIGURE 4: PHYSICAL DIAGRAM**





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# 6. SPECIAL FEATURE

## 6.1. WRITE PROTECT

Netlist CFvault™ II card within the Write-Protect function could prevent the CF card from modification and deletion. Write-Protected data in CF card could only be read, that is, users could not write to it, edit it, append data to it, or delete it.

When users would like to make sure that neither themselves nor others could modify or destroy the file, users could switch on Write-Protection. Thus Netlist CFvault™ II card would process write-protect mechanism and disable flash memory to be written-in any data. Only while the system power-off, users could switch on Write-Protection. Write-protection could not be switched-on, after OS booting.

# 7. RELIABILITY AND DURABILITY

## 7.1. FLASH CONTROLLER

**TABLE 2: FLASH CONTROLLER**

| | | |
|---|---|---|
| **Temperature** | Industrial Operation: -25°C to +85°C<br>Commercial Operation: 0°C to +70°C | |
| **Thermal Shock** | -60°C to 150°C | |
| **Atmospheric Pressure** | Pressure Cooker Test (121°C, 100%RH, 29.7 psi for 168 hours)<br>Highly Accelerated test (130°C, 33.3 psi for 100 hours) | |
| **Vibration** | 15 G peak to peak maximum | |
| **Humidity** | 8% to 95% non-condensing | |
| **ESD Level** | Contact discharge: Up to 8 kV Air discharge: Up to 15kV | |
| **Acoustic Noise** | 0 dB | |
| **Altitude** | 80,000 ft. maximum | |
| **Shock** | 1,500 G | |
| **Power Requirements** | 3.3V +/- 10%<br>Sleep: 300 uA<br>Read: 75 mA<br>Write: 75 mA<br>Read/Write/Peak: 500 mA | 5V +/- 10%<br>Sleep: 500 uA<br>Read: 100 mA<br>Write: 100 mA<br>Read/Write/Peak: 500 mA |

## 7.2. WEAR LEVELING FOR FLASH MEMORY

The Netlist CFvault™ II CompactFlash (CF) Storage Card makes use of the most advanced flash wear leveling and bad block management techniques. Wear leveling is performed with the use of reserved buffer blocks. "Wear leveled" blocks are swapped with replacement blocks that have the fewest erase cycles. Bad block management ensures that defective blocks created during device operation are mapped out and never accessed. In this manner, the life of the entire device is extended.

**TABLE 3: RELIABILITY**

| | |
|---|---|
| **Data Reliability** | <1 non-recoverable error in $10^{14}$ bits read<br><1 erroneous correction in $10^{20}$ bits read |


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# 8. System Performance

**Table 4: Latency Parameters**

| Parameter | Sub-parameter | Value |
|---|---|---|
| **Start Up Times** | Sleep to write | < 0.1 ms |
| | Sleep to read | < 0.1 ms |
| | Reset to ready | < 400 ms |
| **Active to Sleep Delay** | | 20 ms |
| **Controller Overhead** | CMD to DRQ Read<br>CMD to DRQ Write | 0.1 ms |

**Table 5: Data Transfer Rates**

| CMD (Capacity) | Sustained Data-rate[1] |
|---|---|
| Read | Up-to 16 MB/s |
| Write | Up-to 16 MB/s with interleaving |
| Host data transfer rate in PIO mode 6 or MDMA mode 4 | Up to 25 MB/s |
| Host data transfer rate in UDMA mode 4 | Up to 66 MB/s |

# 9. CHS Parameters

**Table 6: CHS Parameters**

| Card Size | Cylinders | Heads | Sectors | Total Sector |
|---|---|---|---|---|
| 128MB | 1,024 | 8 | 32 | 262,144 |
| 256MB | 1,024 | 16 | 32 | 524,288 |
| 512MB | 1,024 | 16 | 63 | 1,032,192 |
| 1,024MB | 1,986 | 16 | 63 | 2,001,888 |
| 2,048MB | 3,970 | 16 | 63 | 4,001,760 |
| 4,096MB | 7,964 | 16 | 63 | 16,007,040 |
| 8,192MB | 31,769 | 16 | 63 | 32,014,080 |
| 16,384MB | 63,538 | 16 | 63 | 64,028,160 |

[1] Based on internal testing on Intel Pentium 4 3.2 GHz, 800 MHz FSB, 512 MB DDR400, Intel 82801EB UATA controller; actual performance may vary on system and environmental factors. Controller frequency @ 55 MHz.

# 10. PIN ASSIGNMENT

**TABLE 7: PIN ASSIGNMENT**

| Pin # | PC Card Memory Mode | | | PC Card I/O Mode | | | True IDE Mode[2] | | |
|---|---|---|---|---|---|---|---|---|---|
| | Signal Name | Pin Type | In, Out Type | Signal Name | Pin Type | In, Out Type | Signal Name | Pin Type | In, Out Type |
| 1 | GND | | Ground | GND | | Ground | GND | | Ground |
| 2 | D03 | I/O | I1Z, OZ[3] | D03 | I/O | I1Z, OZ[3] | D03 | I/O | I1Z, OZ[3] |
| 3 | D04 | I/O | I1Z, OZ[3] | D04 | I/O | I1Z, OZ[3] | D04 | I/O | I1Z, OZ[3] |
| 4 | D05 | I/O | I1Z, OZ[3] | D05 | I/O | I1Z, OZ[3] | D05 | I/O | I1Z, OZ[3] |
| 5 | D06 | I/O | I1Z, OZ[3] | D06 | I/O | I1Z, OZ[3] | D06 | I/O | I1Z, OZ[3] |
| 6 | D07 | I/O | I1Z, OZ[3] | D07 | I/O | I1Z, OZ[3] | D07 | I/O | I1Z, OZ[3] |
| 7 | -CE1 | I | I3U | -CE1 | I | I3U | -CS0 | I | I3Z |
| 8 | A10 | I | I1Z | A10 | I | I1Z | A10[4] | I | I1Z |
| 9 | -OE | I | I3U | -OE | I | I3U | -ATA SEL | I | I3U |
| 10 | A09 | I | I1Z | A09 | I | I1Z | A09[4] | I | I1Z |
| 11 | A08 | I | I1Z | A08 | I | I1Z | A08[4] | I | I1Z |
| 12 | A07 | I | I1Z | A07 | I | I1Z | A07[4] | I | I1Z |
| 13 | $V_{CC}$ | | Power | $V_{CC}$ | | Power | $V_{CC}$ | | Power |
| 14 | A06 | I | I1Z | A06 | I | I1Z | A06[4] | I | I1Z |
| 15 | A05 | I | I1Z | A05 | I | I1Z | A05[4] | I | I1Z |
| 16 | A04 | I | I1Z | A04 | I | I1Z | A04[4] | I | I1Z |
| 17 | A03 | I | I1Z | A03 | I | I1Z | A03[4] | I | I1Z |
| 18 | A02 | I | I1Z | A02 | I | I1Z | A02 | I | I1Z |
| 19 | A01 | I | I1Z | A01 | I | I1Z | A01 | I | I1Z |
| 20 | A00 | I | I1Z | A00 | I | I1Z | A00 | I | I1Z |
| 21 | D00 | I/O | I1Z, OZ[3] | D00 | I/O | I1Z, OZ[3] | D00 | I/O | I1Z, OZ[3] |
| 22 | D01 | I/O | I1Z, OZ[3] | D01 | I/O | I1Z, OZ[3] | D01 | I/O | I1Z, OZ[3] |
| 23 | D02 | I/O | I1Z, OZ[3] | D02 | I/O | I1Z, OZ[3] | D02 | I/O | I1Z, OZ[3] |
| 24 | WP | O | OT3 | -IOIS16 | O | OT3 | -IOCS16 | O | ON3 |
| 25 | -CD2 | O | Ground | -CD2 | O | Ground | -CD2 | O | Ground |
| 26 | -CD1 | O | Ground | -CD1 | O | Ground | -CD1 | O | Ground |
| 27 | D11[5] | I/O | I1Z, OZ[3] | D11[5] | I/O | I1Z, OZ[3] | D11[5] | I/O | I1Z, OZ[3] |

[2] The mode is required for CompactFlash Storage Cards.

[3] The signal should be tied to $V_{CC}$ by the host.

[4] The signal should be grounded by the host.

[5] These signals are required only for 16-bit accesses and not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.



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| Pin # | PC Card Memory Mode | | | PC Card I/O Mode | | | True IDE Mode[2] | | |
|---|---|---|---|---|---|---|---|---|---|
| | Signal Name | Pin Type | In, Out Type | Signal Name | Pin Type | In, Out Type | Signal Name | Pin Type | In, Out Type |
| 28 | D12[5] | I/O | I1Z, OZ[3] | D12[5] | I/O | I1Z, OZ[3] | D12[5] | I/O | I1Z, OZ[3] |
| 29 | D13[5] | I/O | I1Z, OZ[3] | D13[5] | I/O | I1Z, OZ[3] | D13[5] | I/O | I1Z, OZ[3] |
| 30 | D14[5] | I/O | I1Z, OZ[3] | D14[5] | I/O | I1Z, OZ[3] | D14[5] | I/O | I1Z, OZ[3] |
| 31 | D15[5] | I/O | I1Z, OZ[3] | D15[5] | I/O | I1Z, OZ[3] | D15[5] | I/O | I1Z, OZ[3] |
| 32 | -CE2[5] | I | I3U | -CE2[5] | I | I3U | -CS1[5] | I | I3Z |
| 33 | -VS1 | O | Ground | -VS1 | O | Ground | -VS1 | O | Ground |
| 34 | -IORD | I | I3U | -IORD | I | I3U | -IORD7 | I | I3Z |
| | HSTROBE | | | HSTROBE | | | HSTROBE[10] | | |
| | -HDMARDY | | | -HDMARDY | | | -HDMARDY | | |
| 35 | -IOWR | I | I3U | -IOWR | I | I3U | -IOWR[9] | I | I3Z |
| | STOP[6 7] | | | STOP | | | | | |
| 36 | -WE | I | I3U | -WE | I | I3U | -WE | I | I3U |
| 37 | READY | O | OT1 | -IREQ | O | OT1 | INTRQ | O | OZ1 |
| 38 | $V_{CC}$ | | Power | $V_{CC}$ | | Power | $V_{CC}$ | | Power |
| 39 | -CSEL[8] | I | I2Z | -CSEL[8] | I | I2Z | -CSEL | I | I2U |
| 40 | -VS2 | O | OPEN | -VS2 | O | OPEN | -VS2 | O | OPEN |
| 41 | RESET | I | I2Z | RESET | I | I2Z | -RESET | I | I2Z |
| 42 | -WAIT | O | OT1 | -WAIT | O | OT1 | IORDY[9] | O | ON1 |
| | -DDMARDY | | | -DDMARDY | | | -DDMARDY[10] | | OT1[11] |
| | DSTROBE[7] | | | DSTROBE[7] | | | DSTROBE[12] | | |
| 43 | -INPACK | O | OT1 | -INPACK | O | OT1 | DMARQ | O | OZ1 |
| | -DMARQ[13] | | | -DMARQ[13] | | | | | |
| 44 | -REG | I | I3U | -REG | I | I3U | -DMACK | I | I3U |
| | -DMACK[13] | | | DMACK[13] | | | | | |
| 45 | BVD2 | O | OT1 | -SPKR | O | OT1 | -DASP | I/O | I1U, ON[2] |

[6] Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.

[7] Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.

[8] The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

[9] Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.

[10] Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.

[11] Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.

[12] Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

[13] Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.



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| Pin # | PC Card Memory Mode | | | PC Card I/O Mode | | | True IDE Mode[2] | | |
|---|---|---|---|---|---|---|---|---|---|
| | Signal Name | Pin Type | In, Out Type | Signal Name | Pin Type | In, Out Type | Signal Name | Pin Type | In, Out Type |
| 46 | BVD1 | O | OT1 | -STSCHG | O | OT1 | -PDIAG | I/O | I1U, ON[2] |
| 47 | D08[2] | I/O | I1Z, OZ[3] | D08[2] | I/O | I1Z, OZ[3] | D08[2] | I/O | I1Z, OZ[3] |
| 48 | D09[2] | I/O | I1Z, OZ[3] | D09[2] | I/O | I1Z, OZ[3] | D09[2] | I/O | I1Z, OZ[3] |
| 49 | D10[2] | I/O | I1Z, OZ[3] | D10[2] | I/O | I1Z, OZ[3] | D10[2] | I/O | I1Z, OZ[3] |
| 50 | GND | | Ground | GND | | Ground | GND | | Ground |

# 11. SIGNAL DESCRIPTION

**TABLE 8: SIGNAL DESCRIPTION**

| Pin | Dir. | Signal Name | | | Description |
|---|---|---|---|---|---|
| | | PC Card Memory Mode | PC Card IO Mode | True IDE Mode | |
| 8,10,11,12, 14,15,16,17 , 18,19,20 | I | A10 - A00 | | | These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card, the memory mapped port address registers within the CompactFlash Storage Card, a byte in the card's information structure and its configuration control and status registers. |
| | | | A10 - A00 | | This signal is the same as the PC Card Memory Mode signal. |
| 18,19,20 | I | | | A02 - A00 | In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host. |
| 46 | I/O | BVD1 | | | This signal is asserted high, as BVD1 is not supported. |
| | | | -STSCHG | | This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Configuration and Status Register. |
| | | | | Status Changed - PDIAG | In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol. |
| 45 | I/O | BVD2 | | | This signal is asserted high, as BVD2 is not supported. |
| | | | -SPKR | | This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. |
| | | | | -DASP | In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol. |
| 26,25 | O | -CD1, -CD2 | | | These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card is fully inserted into its socket. |
| | | | -CD1, -CD2 | | This signal is the same for all modes. |
| | | | | -CD1, -CD2 | This signal is the same for all modes. |


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| Pin | Dir. | Signal Name | | | Description |
|---|---|---|---|---|---|
| | | PC Card Memory Mode | PC Card IO Mode | True IDE Mode | |
| 7,32 | I | -CE1, -CE2 Card Enable | | | These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8-bit hosts to access all data on D0-D7. While (-) DMACK is asserted, -CE1 and -CE2 shall be held negated and the width of the transfers shall be 16 bits. |
| | | | -CE1, -CE2 Card Enable | | This signal is the same as the PC Card Memory Mode signal. |
| | | | | -CS0, -CS1 Card Enable | In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While -DMACK is asserted, -CS0 and -CS1 shall be held negated and the width of the transfers shall be 16 bits. |
| 39 | I | -CSEL | | | This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. |
| | | | -CSEL | | This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. |
| | | | | -CSEL | This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. |
| 31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21 | I/O | D15 - D00 | | | These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. |
| | | | D15 - D00 | | This signal is the same as the PC Card Memory Mode signal. |
| | | | | D15 - D00 | In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0]. |
| 1,50 | -- | GND | | | Ground. This signal is the same for all This signal is the same for all |
| | | | GND | | Ground. This signal is the same for all This signal is the same for all |


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| Pin | Dir. | Signal Name | | | Description |
|---|---|---|---|---|---|
| | | PC Card Memory Mode | PC Card IO Mode | True IDE Mode | |
| | | | | GND | Ground. This signal is the same for all This signal is the same for all |
| 43 | O | -INPACK | | | This signal is not used in this mode. |
| | | | -INPACK | | The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU.<br>Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the -INPACK signal from the device and manage their input buffers based solely on Card Enable signals. |
| | | | | DMARQ | In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register.<br>While a DMA operation is in progress, -CS0 (-CE1) and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits.<br>If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt to access in DMA mode.<br>A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode. |
| 34 | I | -IORD | | | This signal is not used in this mode. |
| | | | -IORD | | This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface. |
| | | | | -IORD | In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. |
| 35 | I | -IOWR | | | This signal is not used in this mode. |


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| Pin | Dir. | Signal Name | | | Description |
|---|---|---|---|---|---|
| | | PC Card Memory Mode | PC Card IO Mode | True IDE Mode | |
| | | | -IOWR | | The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge). |
| | | | | -IOWR | In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. |
| 9 | I | -OE | | | This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers. This signal should be left floating at power-up to set PC card mode. |
| | | | -OE | | In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. |
| | | | | -ATA SEL | To enable True IDE Mode this input should be grounded by the host. |
| 37 | O | READY | | | In Memory Mode, this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy.<br>At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time.<br>Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. |
| | | | -IREQ | | I/O Operation - After the CompactFlash Storage Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse Mode Interrupt or held low for a level Mode interrupt. |
| | | | | INTRQ | In True IDE Mode signal is the active high Interrupt Request to the host. |


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| Pin | Dir. | Signal Name | | | Description |
|---|---|---|---|---|---|
| | | PC Card Memory Mode | PC Card IO Mode | True IDE Mode | |
| 44 | I | -REG Attribute Memory Select | | | This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device. |
| | | | -REG | | The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device. |
| | | | | -DMACK | A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes. |
| 41 | I | RESET | | | The CompactFlash Storage Card is Reset when the RESET pin is high with the following important exception:<br>The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset.<br>The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. |
| | | | RESET | | This signal is the same as the PC Card Memory Mode signal. |
| | | | | RESET | In the True IDE Mode, this input pin is the active low hardware reset from the host. |
| 13,38 | -- | $V_{CC}$ | | | +5 V, +3.3 V power. This signal is the same for all. |
| | | | $V_{CC}$ | | +5 V, +3.3 V power. This signal is the same for all. |
| | | | | $V_{CC}$ | +5 V, +3.3 V power. This signal is the same for all. |
| 33, 40 | O | -VS1 -VS2 | | | Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card CIS can be read at 3.3 volts. -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. |

| Pin | Dir. | Signal Name | | | Description |
|---|---|---|---|---|---|
| | | PC Card Memory Mode | PC Card IO Mode | True IDE Mode | |
| | | | -VS1 -VS2 | | This signal is the same for all modes. |
| | | | | -VS1 -VS2 | This signal is the same for all modes. |
| 42 | O | -WAIT | | | The -WAIT signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress. |
| | | | -WAIT | | This signal is the same as the PC Card Memory Mode signal. |
| | | | | IORDY | In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. |
| 36 | I | -WE | | | This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. |
| | | | -WE | | In PC Card I/O Mode, this signal is used for writing the configuration registers. |
| | | | | -WE | In True IDE Mode, this input signal is not used and should be connected to $V_{CC}$ by the host. |
| 24 | O | WP | | | Memory Mode - The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. |
| | | | -IOIS16 | | I/O Operation - When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16-bit or odd byte only operation can be performed at the addressed port. |
| | | | | -IOCS16 | In True IDE Mode, this output signal is asserted low when this device is expecting a word data transfer cycle. |

# 12. DC CHARACTERISTICS

Following Tables define all D.C. Characteristics for the CF Storage Card using the conditions listed below.

VCC = 5V ±10%; VCC = 3.3V ± 5%;

**TABLE 9: ABSOLUTE MAXIMUM CONDITIONS**

| Parameter | Symbol | Conditions |
|---|---|---|
| Operating Temperature Range | $T_{AMB}$ | 0°C to +85°C |
| Input Power | $V_{CC}$ | -0.3V min. to 6.5V max. |
| Voltage on any pin except $V_{CC}$ with respect to GND. | V | -0.5V min. to $V_{CC}$ + 0.5V max. |

**TABLE 10: INPUT POWER**

| Voltage | Maximum Average RMS Current | Measurement Method | |
|---|---|---|---|
| Power Level 0 | Power Level 1 | | |
| 3.3V ± 5% | 75 mA | 500 mA | 3.3V -25°C |
| 5.0V ± 10% | 100 mA | 500 mA | 5.0V -25°C |

**TABLE 11: INPUT LEAKAGE CURRENT**

| Type | Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| IxZ | Input Leakage Current | IL | Vih = $V_{CC}$<br>Vil = Gnd | -1 | 1 | µA |
| IxU | Pull-Up Resistor | RPU1 | $V_{CC}$ = 5.0V | 50k | 500k | Ohm |
| IxD | Pull-Down Resistor | RPD1 | $V_{CC}$ = 5.0V | 50k | 500k | Ohm |

**TABLE 12: INPUT CHARACTERISTICS**

| Type | Parameter | Symbol | Min | TYP | Max | Min | TYP | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V | | | $V_{CC}$= 5.0 V | | | |
| 1 | Input Voltage CMOS | Vih Vil | 2.4 | | 0.6 | 4.0 | | 0.8 | Volts |
| 2 | Input Voltage CMOS | Vih Vil | 1.5 | | 0.6 | 2.0 | | 0.8 | Volts |
| 3 | Input Voltage CMOS Schmitt Trigger | Vth Vtl | | 1.8 1.0 | | | 2.8 2.0 | | Volts |

**TABLE 13: OUTPUT DRIVE TYPE**

| Type | Output Type | Valid Conditions |
|---|---|---|
| OTx | Totempole | Ioh & Iol |
| OZx | Tri-State N-P Channel | Ioh & Iol |
| OPx | P-Channel Only | Ioh Only |
| ONx | N-Channel Only | Iol Only |


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**TABLE 14: OUTPUT DRIVE CHARACTERISTICS**

| Type | Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| 1 | Output Voltage | Voh<br>Vol | Ioh = -4 mA<br>Iol = 4 mA | $V_{CC}$ -0.8V | Gnd +0.4V | Volts |
| 2 | Output Voltage | Voh<br>Vol | Ioh = -4 mA<br>Iol = 4 mA | $V_{CC}$ -0.8V | Gnd +0.4V | Volts |
| 3 | Output Voltage | Voh<br>Vol | Ioh = -4 mA<br>Iol = 4 mA | $V_{CC}$ -0.8V | Gnd +0.4V | Volts |
| X | Tri-State Leakage Current | Ioz | Voh = $V_{CC}$<br>Vol = Gnd | -10 | 10 | µA |


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# 13. AC CHARACTERISTICS

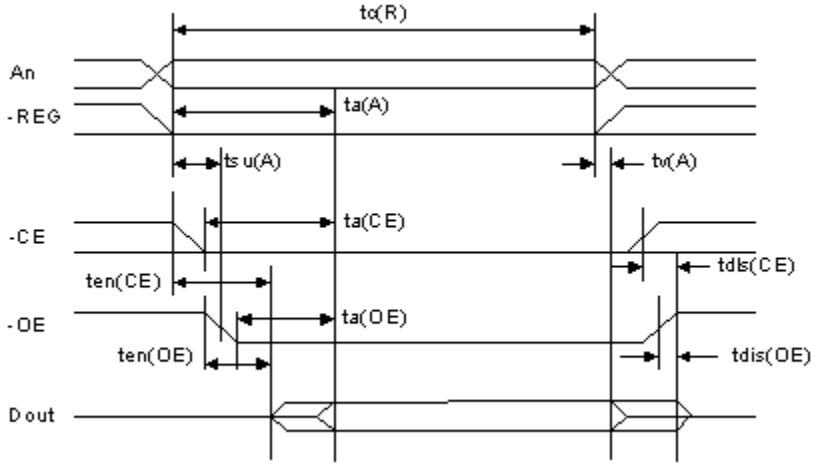
There are two types of bus cycles and timing sequences that occur in the PC Card type interface, direct mapped I/O transfer and memory access. The two timing sequences are detailed in the PCMCIA PC Card Standard. The CompactFlash Storage Card will conform to the timing in that reference document.

Attribute Memory access time is defined as 300 ns. Detailed timing specs are shown below.

**TABLE 15: ATTRIBUTE MEMORY READ TIMING SPECIFICATION (PCMCIA MODE)**

| Speed Version | | | 300 ns | |
|---|---|---|---|---|
| **Item** | **Symbol** | **IEEE Symbol** | **Min ns.** | **Max ns.** |
| Read Cycle Time | tc(R) | tAVAV | 300 | |
| Address Access Time | ta(A) | tAVQV | | 300 |
| Card Enable Access Time | ta(CE) | tELQV | | 300 |
| Output Enable Access Time | ta(OE) | tGLQV | | 150 |
| Output Disable Time from CE | tdis(CE) | tEHQZ | | 100 |
| Output Disable Time from OE | tdis(OE) | tGHQZ | | 100 |
| Address Setup Time | tsu (A) | tAVGL | 30 | |
| Output Enable Time from CE | ten(CE) | tELQNZ | 5 | |
| Output Enable Time from OE | ten(OE) | tGLQNZ | 5 | |
| Data Valid from Address Change | tv(A) | tAXQX | 0 | |

**FIGURE 5: ATTRIBUTE MEMORY READ TIMING SPECIFICATION (PCMCIA MODE)**





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The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown below.

**TABLE 16: ATTRIBUTE MEMORY WRITE TIMING (PCMCIA MODE)**

| Speed | | | |
|---|---|---|---|
| **Item** | **Symbol** | **IEEE Symbol** | **ns** |
| Write Cycle Time | tc(W) | tAVAV | 250 |
| Write Pulse Width | tw(WE) | tWLWH | 150 |
| Address Setup Time | tsu(A) | tAVWL | 30 |
| Write Recovery Time | trec(WE) | tWMax | 30 |
| Data Setup Time for WE | tsu(D-WEH) | tDVWH | 80 |
| Data Hold Time | th(D) | tWMDX | 30 |

**FIGURE 6: ATTRIBUTE MEMORY WRITE TIMING (PCMCIA MODE)**

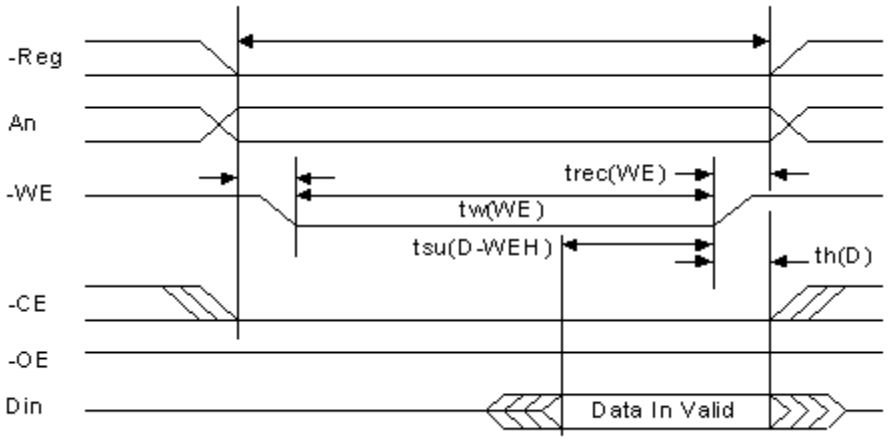



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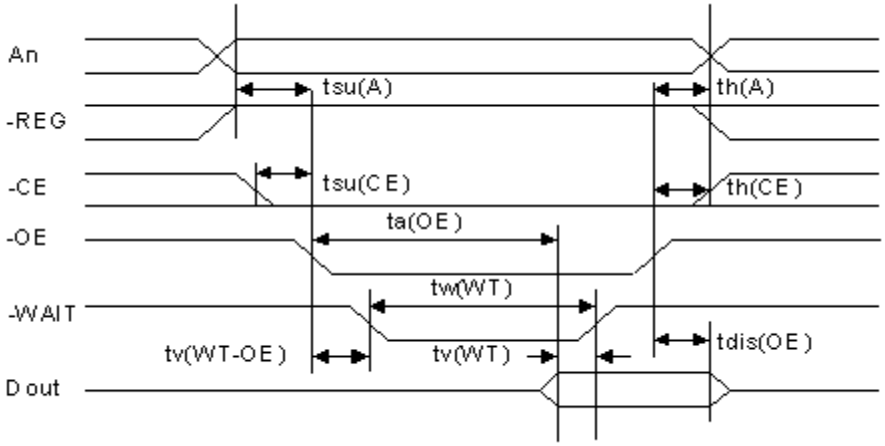
**TABLE 17: COMMON MEMORY READ TIMING SPECIFICATION (PCMCIA MODE)**

| Cycle Time Mode: | | | 250 ns | | 120 ns | | 100 ns. | | 80 ns | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **IEEE Symbol** | **Min (ns)** | **Max (ns)** | **Min (ns)** | **Max (ns)** | **Min (ns)** | **Max (ns)** | **Min (ns)** | **Max (ns)** |
| Output Enable Access Time | ta(OE) | tGLQV | | 125 | | 60 | | 50 | | 45 |
| Output Disable Time from OE | tdis(OE) | tGHQZ | | 100 | | 60 | | 50 | | 45 |
| Address Setup Time | tsu(A) | tAVGL | 30 | | 15 | | | | 10 | |
| Address Hold Time | th(A) | tGHAX | 20 | | 15 | | | | 10 | |
| CE Setup before OE | tsu(CE) | tELGL | 0 | | 0 | | | | 0 | |
| CE Hold following OE | th(CE) | tGHEH | 20 | | 15 | | | | 10 | |
| Wait Delay Falling from OE | tv(WT-OE) | tGLWTV | | 35 | | 35 | | 35 | | na[14] |
| Data Setup for Wait Release | tv(WT) | tQVWTH | | 0 | | 0 | | 0 | | na[14] |
| Wait Width Time[15] | tw(WT) | tWTLWTH | | 350 | | 350 | | 350 (3000 for CF+) | | na[14] |

**FIGURE 7: COMMON MEMORY READ TIMING SPECIFICATION (PCMCIA MODE)**



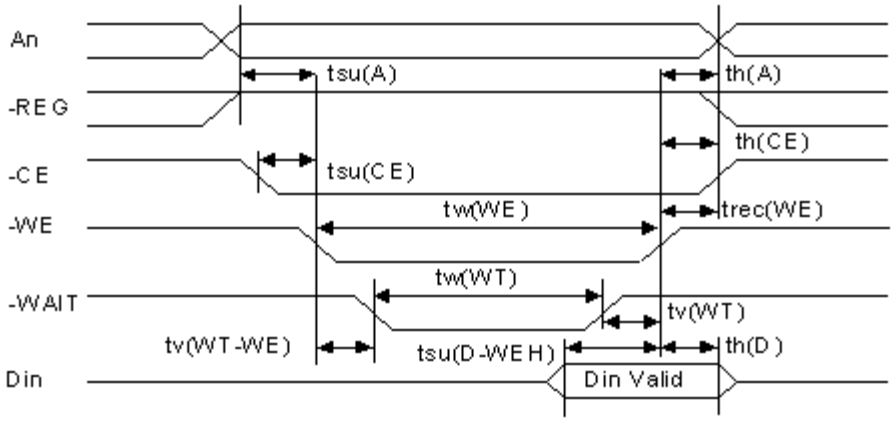

[14] WAIT is not supported in this mode.

[15] The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12ìs but is intentionally less in this specification.

**TABLE 18: COMMON MEMORY WRITE TIMING (PCMCIA MODE)**

| Cycle Time Mode | | | 250 ns | | 120 ns | | 100 ns | | 80 ns | |
|---|---|---|---|---|---|---|---|---|---|---|
| Item | Symbol | IEEE Symbol | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) |
| Data Setup before WE | tsu (D-WEH) | tDVWH | 80 | | 50 | | 40 | | 30 | |
| Data Hold following WE | th(D) | tWMDX | 30 | | 15 | | 10 | | 10 | |
| WE Pulse Width | tw(WE) | tWLWH | 150 | | 70 | | 60 | | 55 | |
| Address Setup Time | tsu(A) | tAVWL | 30 | | 15 | | 10 | | 10 | |
| CE Setup before WE | tsu(CE) | tELWL | 0 | | 0 | | 0 | | 0 | |
| Write Recovery Time | trec(WE) | tWMax | 30 | | 15 | | 15 | | 15 | |
| Address Hold Time | th(A) | tGHAX | 20 | | 15 | | 15 | | 15 | |
| CE Hold following WE | th(CE) | tGHEH | 20 | | 15 | | 15 | | 10 | |
| Wait Delay Falling from WE | tv (WT-WE) | tWLWTV | | 35 | | 35 | | 35 | | na[16] |
| WE High from Wait Release | tv(WT) | tWTHWH | 0 | | 0 | | 0 | | na[16] | |
| Wait Width Time[17] | tw (WT) | tWTLWTH | | 350 | | 350 | | 350 (3000 for CF+) | | na[16] |

**FIGURE 8: COMMON MEMORY WRITE TIMING (PCMCIA MODE)**




[16] WAIT is not supported in this mode.

[17] The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12ìs but is intentionally less in this specification.



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# 14. TRUE IDE PIO MODE READ/WRITE TIMING

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different from the conventions used in the PCMCIA PC Card specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

**TABLE 19: TRUE IDE PIO MODE READ/WRITE TIMING**

| | Item | Mode | | | | | |
|---|---|---|---|---|---|---|---|
| | | **0** | **1** | **2** | **3** | **4** | **6** |
| t0 | Cycle time (min) | 600 | 383 | 240 | 180 | 120 | 80 |
| t1 | Address Valid to -IORD/-IOWR setup (min) | 70 | 50 | 30 | 30 | 25 | 10 |
| t2 | -IORD/-IOWR (min) | 165 | 125 | 100 | 80 | 70 | 55 |
| t2 | -IORD/-IOWR (min) Register (8 bit) | 290 | 290 | 290 | 80 | 70 | 55 |
| t2i | -IORD/-IOWR recovery time (min) | - | - | - | 70 | 25 | 20 |
| t3 | -IOWR data setup (min) | 60 | 45 | 30 | 30 | 20 | 15 |
| t4 | -IOWR data hold (min) | 30 | 20 | 15 | 10 | 10 | 5 |
| t5 | -IORD data setup (min) | 50 | 35 | 20 | 20 | 20 | 10 |
| t6 | -IORD data hold (min) | 5 | 5 | 5 | 5 | 5 | 5 |
| T6Z | -IORD data tristate (max) | 30 | 30 | 30 | 30 | 30 | 20 |
| t7 | Address valid to -IOCS16 assertion (max) | 90 | 50 | 40 | n/a | n/a | n/a |
| t8 | Address valid to -IOCS16 released (max) | 60 | 45 | 30 | n/a | n/a | n/a |
| t9 | -IORD/-IOWR to address valid hold | 20 | 15 | 10 | 10 | 10 | 10 |
| tRD | Read Data Valid to IORDY active (min), if IORDY initially low after tA | 0 | 0 | 0 | 0 | 0 | 0 |
| tA | IORDY Setup time | 35 | 35 | 35 | 35 | 35 | n/a |
| tB | IORDY Pulse Width (max) | 1250 | 1250 | 1250 | 1250 | 1250 | n/a |
| tC | IORDY assertion to release (max) | 5 | 5 | 5 | 5 | 5 | n/a |


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**TABLE 20: TRUE IDE MULTIWORD DMA MODE READ/WRITE TIMING**

| | Item | Mode 0 (ns) | Mode 1 (ns) | Mode 2 (ns) | Mode 4 (ns) |
|---|---|---|---|---|---|
| tO | Cycle time (min) | 480 | 150 | 120 | 80 |
| tD | -IORD / -IOWR asserted width (min) | 215 | 80 | 70 | 55 |
| tE | -IORD data access (max) | 150 | 60 | 50 | 45 |
| tF | -IORD data hold (min) | 5 | 5 | 5 | 5 |
| tG | -IORD/-IOWR data setup (min) | 100 | 30 | 20 | 10 |
| tH | -IOWR data hold (min) | 20 | 15 | 10 | 5 |
| tI | DMACK to -IORD/-IOWR setup (min) | 0 | 0 | 0 | 0 |
| tJ | -IORD / -IOWR to -DMACK hold (min) | 20 | 5 | 5 | 5 |
| tKR | -IORD negated width (min) | 50 | 50 | 25 | 20 |
| tKW | -IOWR negated width (min) | 215 | 50 | 25 | 20 |
| tLR | -IORD to DMARQ delay (max) | 120 | 40 | 35 | 35 |
| tLW | -IOWR to DMARQ delay (max) | 40 | 40 | 35 | 35 |
| tM | CS(1:0) valid to -IORD / -IOWR | 50 | 30 | 25 | 5 |
| tN | CS(1:0) hold | 15 | 10 | 10 | 10 |
| tZ | -DMACK | 20 | 25 | 25 | 25 |


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# 15. CARD CONFIGURATION

The CompactFlash Storage Cards are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

Please refer to the Appendix III for complete information of the CIS offsets, content and functions.

(Note - Offsets 01Eh - CISTPL_MANFID & offset 12Ah-CISTPL_VERS_1 reflect Netlist)

The host can access the CompactFlash Card in the following modes:

## 15.1. PCMCIA MEMORY MODE

For the Attribute Memory Read function, signals -REG and -OE shall be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access.

## 15.2. ATTRIBUTE MEMORY FUNCTION

Attribute memory is a space where CompactFlash Storage Card identification and configuration information are stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the card configuration registers is 200h.

## 15.3. COMMON MEMORY FUNCTION

The Common Memory can be accessed in the Byte/Word/Odd Byte modes in PC Card Memory Mode. The -REG signal must be de-asserted when accessing the Common Memory. The CF Card is mapped to PC Card Memory Mode by the Index bits in the Configuration Option Register. The Common Memory transfer to or from the CompactFlash Storage Card can be either 8 or 16 bits. The CompactFlash Storage Card permits both 8 and 16-bit accesses to all of its Common Memory addresses. The CompactFlash Storage Card or the CF+ Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

## 15.4. PCMCIA IO MODE

The CompactFlash Card can be accessed by Byte/Word/Odd Byte modes in PC Card I/O Mode. The CF Card is mapped to PC Card I/O Mode by the Index bits in the Configuration Option Register. The index bits also select Contiguous I/O, Primary I/O, or Secondary I/O mapping when using the PC Card I/O Mode.

## 15.5. TRUE IDE MODE I/O TRANSFER FUNCTION

The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards may support the following optional detection methods:

The card is permitted to monitor the -OE (-ATA SEL) signal at any time(s) and switch to PC Card mode upon detecting a high level on the pin.

The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin.

The card is permitted to monitor the -OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time.

(In this mode, no Memory or Attribute Registers are accessible to the host. CompactFlash Storage Cards permit 8 bit PIO mode data accesses if the user issues a Set Feature Command to put the CompactFlash Storage Card in 8 bit Mode.)

# 16. CONFIGURATION REGISTERS IN THE ATTRIBUTE MEMORY

**TABLE 21: CONFIGUATION REGISTERS IN THE ATTRIBUTE MEMORY**

| Name | Description |
|---|---|
| Configuration Option Register (Base + 00h in Attribute Memory) | The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Storage Card. |
| Card Configuration and Status Register (Base + 02h in Attribute Memory) | The Card Configuration and Status Register contain information about the Card's condition. |
| Pin Replacement Register (Base + 04h in Attribute Memory) | This register is used for providing the signal state of -IREQ when the CF Card is configured in the PC Card I/O Mode. |
| Socket and Copy Register (Base + 06h in Attribute Memory) | This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is not required for CFs. If present, it is optional for a CF Card to allow setting bit D4 (Drive number) to 1. If two drives are supported, it is intended for use only when two cards are co-located at either the primary or the secondary addresses in PC Card I/O mode. The availability and capabilities of this register are described in the Card Information Structure of the CF Card. |

# 17. CF-ATA DRIVE REGISTER SET DEFINITION AND PROTOCOL

The CompactFlash Storage Card can be configured as a high performance I/O device through the addressing modes mentioned below. The communication to or from the CompactFlash Storage Card is done using the Task File registers, which provide all the necessary registers for control and status information related to the storage medium.

## 17.1. ADDRESSING MODES

**TABLE 22: ADDRESSING MODES**

| Name | Description |
|---|---|
| Memory Mapped Addressing | When the CompactFlash Storage Card registers are accessed via memory references, the registers appear in the common memory space window of 0-2K bytes. |
| Standard IO Addressing | In this mode the CompactFlash Storage Card Registers can be accessed via the standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary) or 170h- 177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ). |
| True IDE Mode Addressing | The CompactFlash Storage Card is configured in the True IDE Mode using any system decoded 16-byte I/O block using any available IRQ. |


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## 17.2. CF-ATA TASK-FILE REGISTERS

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file." (Note: In accordance with the PCMCIA PC Card specification: each of the registers below that is located at an odd offset address may be accessed in the PC Card Memory or PC Card I/O modes at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted by the card) and an I/O cycle is being performed. In the True IDE mode of operation, the size of the transfer is based solely on the register being addressed. All registers are 8 bit only except for the Data Register, which is normally 16 bits, but can be programmed to use 8-bit transfers for Non-DMA operations using the Set Features command. The data register is also 8 bits during a portion of the Read Long and Write Long commands, which exist solely for historical reasons and should not be used.)

**TABLE 23: CF-ATA TASK-FILE REGISTERS**

| Name | Description | |
|---|---|---|
| **Data Register** | The Data Register is a 16-bit register, and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register. Data Register Access below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA PC Card word and byte access modes and operations. See the PCMCIA PC Card Standard, for further definitions of the Card Accessing Modes for I/O and Memory cycles. | |
| **Error Register** | This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. | |
| **Feature Register** | This register provides information regarding features of the CompactFlash Storage Card that the host can utilize. This register is also accessed in PC Card modes on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high. | |
| **Sector Count Register** | This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request. | |
| **Sector Number** | This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Storage Card data access for the subsequent command. | |
| **Cylinder Low** | This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address. | |
| **Cylinder High** | This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address | |
| **Drive/Head** | The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. | |
| **Status & Alternate Status Registers** | These registers return the CompactFlash Storage Card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The status bits are described as follows: | |
| | **Device Control Register** | This register is used to control the CompactFlash Storage Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. |


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| Name | Description | |
|---|---|---|
| | **Card (Drive) Address Register** | This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. |

# 18. CF-ATA COMMAND SET

This section defines the software requirements and commands the host sends to the CompactFlash Storage Cards. Commands are issued to the CompactFlash Storage Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 48: CF-ATA Command Set) of command acceptance, all dependent on the host not issuing commands unless the CompactFlash Storage Card is not busy (BSY=0). All commands listed in this specification shall be implemented. Commands can be implemented as "no operation" to meet this requirement. The Security Mode feature set (command codes F1, F2, F3, F4, F5, and F6) should not be implemented unless the device is intended to be used in an embedded, non-removable application. The Security Mode feature set was not designed for removable devices and certain problems may be encountered when using these commands in a removable application. This specification introduces some new commands and features. If these commands are used on an older CF card, an Invalid Command Error may occur.

Upon receipt of a Class 1 command, the CompactFlash Storage Card sets BSY within 400 ns.

Upon receipt of a Class 2 command, the CompactFlash Storage Card sets BSY within 400 ns, sets up the sector buffer for a write operation, sets DRQ within 700 ms, and clears BSY within 400 ns of setting DRQ.

Upon receipt of a Class 3 command, the CompactFlash Storage Card sets BSY within 400 ns, sets up the sector buffer for a write operation, sets DRQ within 20 ms (assuming no re-assignments), and clears BSY within 400 ns of setting DRQ.

CF-ATA Command Set summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each. For further description of the commands, please refer to the CompactFlash Association Specification for "CF+ and CompactFlash Specification, Revision 4".

**TABLE 24: COMMAND SET**

| No. | Class | Command Set | Code | FR | SC | SN | CY | DH | LBA |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | Check Power Mode | E5H, 98H | - | - | - | - | D | - |
| 2 | 1 | Execute Drive Diagnostic | 90H | - | - | - | - | D | - |
| 3 | 1 | Erase Sector(s) | C0H | - | Y | Y | Y | Y | Y |
| 4 | 2 | Format Track | 50H | - | Y | - | Y | Y | Y |
| 5 | 1 | Identify Device | ECH | - | - | - | - | D | - |
| 6 | 1 | Idle | E3H, 97H | - | Y | - | - | D | - |
| 7 | 1 | Idle Immediate | E1H, 95H | - | - | - | - | D | - |
| 8 | 1 | Initialize Drive Parameters | 91H | - | Y | - | - | Y | - |
| 9 | 1 | NOP | 00h | - | - | - | - | D | - |
| 10 | 1 | Read Buffer | E4H | - | - | - | - | D | - |
| 11 | 1 | Read DMA | C8h | - | Y | Y | Y | Y | Y |
| 12 | 1 | Read Multiple | C4H | - | Y | Y | Y | Y | Y |
| 13 | 1 | Read Long Sector | 22H, 23H | - | - | Y | Y | Y | Y |
| 14 | 1 | Read Sector(s) | 20H, 21H | - | Y | Y | Y | Y | Y |
| 15 | 1 | Read Verify Sector(s) | 40H, 41H | - | Y | Y | Y | Y | Y |
| 16 | 1 | Recalibrate | 1XH | - | - | - | - | D | - |
| 17 | 1 | Request Sense | 03H | - | - | - | - | D | - |
| 18 | 1 | Seek | 7XH | - | - | Y | Y | Y | Y |
| 19 | 1 | Set Features | EFH | Y | - | - | - | D | - |
| 20 | 1 | Set Multiple Mode | C6H | - | Y | - | - | D | - |
| 21 | 1 | Set Sleep Mode | E6H, 99H | - | - | - | - | D | - |
| 22 | 1 | Stand By | E2H, 96H | - | - | - | - | D | - |
| 23 | 1 | Stand By Immediate | E0H, 94H | - | - | - | - | D | - |
| 24 | 1 | Translate Sector | 87H | - | Y | Y | Y | Y | Y |
| 25 | 1 | Wear Level | F5H | - | - | - | - | Y | - |
| 26 | 2 | Write Buffer | E8H | - | - | - | - | D | - |
| 27 | 2 | Write DMA | CAh | - | Y | Y | Y | Y | Y |
| 28 | 2 | Write Long Sector | 32H, 33H | - | - | Y | Y | Y | Y |
| 29 | 3 | Write Multiple | C5H | - | Y | Y | Y | Y | Y |
| 30 | 3 | Write Multiple w/o Erase | CDH | - | Y | Y | Y | Y | Y |
| 31 | 3 | Write Sector(s) | 30H, 31H | - | Y | Y | Y | Y | Y |
| 32 | 3 | Write Sector(s) w/o Erase | 38H | - | Y | Y | Y | Y | Y |
| 33 | 3 | Write Verify | 3CH | - | Y | Y | Y | Y | Y |


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**TABLE 25: IDENTIFY DEVICE INFORMATION**

| Word Address | Default Value (Hex) | Bytes | Data Field Type Information |
|---|---|---|---|
| 0 | 848A | 2 | General configuration bit-significant information |
| 1 | XXXX | 2 | Default number of cylinders |
| 2 | 0000 | 2 | Reserved |
| 3 | 00XX | 2 | Default number of heads |
| 4 | 0000 | 2 | Number of unformatted bytes per track |
| 5 | 0200 | 2 | Number of unformatted bytes per sector |
| 6 | XXXX | 2 | Default number of sectors per track |
| 7 to 8 | XXXX | 4 | Number of sectors per card |
| 9 | 0000 | 2 | Reserved |
| 10 | XXXX | 2 | Manufacturer |
| 11 | 2D | 1 | Product Type |
| | 41 | 1 | Flash Manufacturer |
| 12 | 44 | 1 | Flash Architecture (“D” - Dual Plane) |
| | 55 | 1 | DMA Support (“U” - Ultra DMA Enabled) |
| 13 | 41 | 1 | Feature Set (“A” - Auto Detect) |
| | xx | 1 | Capacity (GB) |
| 14 | 32 | 1 | Number of channels (“2” - Dual channel) |
| | 00 | 1 | Customer designator |
| 15 | 00 | 1 | Customer designator |
| | 20 | 1 | space |
| 16 | 31 | 1 | Manufacturing Year (“1” - 2011) |
| | 32 | 1 | Test Station Number (“2” - Station 2) |
| 17 to 19 | 303030303031 | 6 | ESN (start from 000001 and increments) |
| 20 | 0001 | 2 | Buffer type (single ported) |
| 21 | 0001 | 2 | Buffer size in 512 byte increments |
| 22 | 0004 | 2 | # ECC bytes passed on Read/Write Long Commands |
| 23 to 26 | 362f31332f3037 | 8 | Firmware revision (8 ASCII characters) - "4/14/08" |


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| Word Address | Default Value (Hex) | Bytes | Data Field Type Information |
|---|---|---|---|
| 27 to 46 | 4e65746c69737420466c6173682076312e30 | 40 | Model Number (40 ASCII characters) - "Netlist Flash v2.0" |
| 47 | 0001 | 2 | Maximum of 1 sector on Read/Write Multiple command |
| 48 | 0000 | 2 | Double Word not supported |
| 49 | 0300 | 2 | Capabilities: DMA Supported, LBA supported |
| 50 | 0000 | 2 | Reserved |
| 51 | 0200 | 2 | PIO data transfer cycle timing mode 2 |
| 52 | 0000 | 2 | DMA data transfer cycle timing mode not Supported |
| 53 | 0001 | 2 | Data Fields 54 to 58 are valid |
| 54 | XXXX | 2 | Number of current logical cylinders |
| 55 | XXXX | 2 | Number of current logical heads |
| 56 | XXXX | 2 | Number of current logical sectors per track |
| 57 to 58 | XXXX | 4 | Current Capacity in sectors |
| 59 | 010X | 2 | Multiple sector setting is valid |
| 60 to 61 | XXXX | 4 | Total number of sectors addressable in LBA Mode |
| 62 to 255 | 0000 | 388 | Reserved |


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# 19. APPENDIX I (STANDARDS AND SPECIFICATIONS)

Copies of the following PCMCIA standards can be obtained from:

2635 North First St., Ste. 209
San Jose, CA 95131 USA

Phone: 408-433-2273
Fax: 408-433-9558

Copies of the following ATA standards can be purchased from:

ANSI or Global Engineering Documents
11 West 42nd Street Inverness Way East
New York, NY 10036 USA Englewood, CO 80112-5704

Tel: 212 642-4900
Tel: 800 854-7179

Outside USA and Canada 303 792-2181
International Sales Fax: 303 397-2740.

# 20. APPENDIX II (CIS)

**TABLE 26: APPENDIX II (CIS)**

| Address | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 000H | 01H | CISTPL_DEVICE | | | | | | | | Device info tuple | Tuple code |
| 002H | 03H | TPL_LINK | | | | | | | | Link length is 3 byte | Link to next tuple |
| 004H | D9H | Device Type | | | | W | Speed | | | Type = D:I/O device<br>WPS = 1:no W switch<br>Speed = 1: 250ns | Device type, WPS, speed |
| 006H | 01H | #address units-1 | | | | | unit size | | | 2 Kbytes of address space | Device size |
| 008H | FFH | CISTPL_END | | | | | | | | End of CISTPL_DEVICE | End marker |
| 00AH | 1Ch | CISTPL_DEVICE_OC | | | | | | | | Common memory other operating conditions tuple | Tuple code |
| 00CH | 04H | TPL_LINK | | | | | | | | Link length is 4 byte | Link to next tuple |
| 00EH | 02H | Ext Reserved | | | | | | 3V | M | 3V = 1: dual voltage card, conditions for 3.3V operation M=0: conditions without wait | Other Conditions information |
| 010H | D9H | Device Type | | | | W | Speed | | | Type = D:I/O device<br>WPS = 1:no W switch<br>Speed = 1: 250ns | Device type, WPS, speed |
| 012H | 01H | #address units-1 | | | | | unit size | | | 2 Kbytes of address space | Device size |
| 014H | FFH | CISTPL_END | | | | | | | | End of CISTPL_DEVICE_OC | End marker |
| 016H | 18H | CISTPL_JEDEC_C | | | | | | | | JEDEC programming info tuple | Tuple code |
| 018H | 02H | TPL_LINK | | | | | | | | Link length is 2 byte | Link to next tuple |
| 01AH | DFH | JEDEC ID | | | | | | | | Device manufacturer ID | Manufacturer ID |
| 01CH | 01H | JEDEC Info | | | | | | | | Manufacturer specific ID | Manufacturer info |
| 01EH | 20H | CISTPL_MANFID | | | | | | | | manufacturer ID tuple | Tuple code |
| 020H | 04H | TPL_LINK | | | | | | | | Link length is 4 bytes | Link to next tuple |
| 022H | 00H | TPLMID_MANF | | | | | | | | PC Card manufacturer code | Manufacturer ID |
| 024H | 00H | | | | | | | | | | |
| 026H | 00H | TPLMID_CARD | | | | | | | | Manufacturer specific info | Manufacturer info |
| 028H | 00H | | | | | | | | | | |
| 02AH | 21H | CISTPL_FUNCID | | | | | | | | Function ID tuple | Tuple code |
| 02CH | 02H | CISTPL_LINK | | | | | | | | Link length is 2 byte | Link to next tuple |
| 02EH | 04H | TPLFID_FUNCTION | | | | | | | | Fixed disk drive | Function code |
| 030H | 01H | Reserved | | | | | | R | P | R=0: no expansion ROM<br>P=1: configure at POST | System init byte<br>TPLFID_SYSINIT |
| 032H | 22H | CISTPL_FUNCE | | | | | | | | Function Extension tuple | Tuple code |
| 034H | 02H | CISTPL_LINK | | | | | | | | Link length is 2 byte | Link to next tuple |
| 036H | 01H | Disk function extension tuple | | | | | | | | Disk interface information | TPLFE_TYPE |
| 038H | 01H | Disk interface type | | | | | | | | PC card ATA interface | TPLFE_DATA |
| 03AH | 22H | CISTPL_FUNCE | | | | | | | | Function Extension tuple | Tuple code |
| 03CH | 03H | CISTPL_LINK | | | | | | | | Link length is 3 byte | Link to next tuple |


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| Address | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 03EH | 02H | Disk function extension tuple | | | | | | | | PC card ATA basic features | TPLFE_TYPE |
| 040H | 04H | Reserved | | | D | U | S | V | | D=0: single drive on card<br>U=0: no unique serial number<br>S=1: silicon device<br>V=0 no $V_{PP}$ required | TPLFE_TYPE |
| 042H | 07H | R | I | E | N | P | | | | I=0: twin IOIS16# unspecified<br>E=0: index bit not emulated<br>N=0: I/O includes 0x3F7<br>P=7: sleep, standby, idle supported | TPLFE_TYPE |
| 044H | 1AH | CISTPL_CONFIG | | | | | | | | Configuration Tuple | Tuple code |
| 046H | 05H | TPL_LINK | | | | | | | | Link length is 5 bytes | Link to next tuple |
| 048H | 01H | RFS | | RMS | | | | RAS | | RFS: reserved<br>RMS: 1 byte register mask<br>RAS: 2 bytes base address | Size of fields TPCC_SZ |
| 04AH | 07H | TPCC_LAST | | | | | | | | Last configuration entry is 07H | Last entry index |
| 04CH | 00H | TPCC_RADAR (LSB) | | | | | | | | Configuration registers are located at 0200H | Configuration register location |
| 04EH | 02H | TPCC_RADAR (MSB) | | | | | | | | | |
| 050H | 0FH | TPCC_RMSK | | | | | | | | Configuration registers 0 to 3 are present | Configuration register present mask |
| 052H | 1BH | CISTPL_CFTABLE_ENTRY | | | | | | | | Configuration tuple | Tuple code |
| 054H | 0BH | CISTPL_LINK | | | | | | | | Link length is 11 bytes | Link to next tuple |
| 056H | C0H | I | D | Configuration Index | | | | | | Memory mapped configuration index = 0<br>I=1: Interface byte follows<br>D=1: Default entry | Configuration Table Index Byte TPCE_INDX |
| 058H | C0H | W | R | P | B | Interface type | | | | W=1: wait required<br>R=1: ready/busy active<br>P=0: WP not used<br>B=0:BVD1, BVD2 not used<br>Type=0: Memory interface | Interface Description TPCE_IF |
| 05AH | A1H | M | MS | | IR | IO | T | Power | | M=1: misc info present<br>MS=1: 2 byte memory length<br>IR=0: no interrupt is used<br>IO=0: no I/O space is used<br>T=0: no timing info specified<br>Power=1: $V_{CC}$ info, no $V_{PP}$ | Feature Selection Byte TPCE_FS |
| 05CH | 27H | R | DI | PI | AI | SI | HV | LV | NV | DI: no power-down current<br>PI=1: peak current info<br>AI: no average current info<br>SI: no static current info<br>HV=1: max voltage info<br>LV=1: min voltage info<br>NV=1: nominal voltage info | Power Description Structure Parameter Selection Byte TPCE_PD |
| 05EH | 55H | X | Mantissa | | | | Exponent | | | Nominal voltage 5.0V | |
| 060H | 4DH | X | Mantissa | | | | Exponent | | | Minimum voltage 4.5V | |
| 062H | 5DH | X | Mantissa | | | | Exponent | | | Maximum voltage 5.5V | |


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| Address | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 064H | 75H | X | Mantissa | | | | Exponent | | | Peak current 80 mA | |
| 066H | 08H | Length in 256 byte units (LSB) | | | | | | | | Length of memory is 2 Kbytes | Memory space descr.<br>TPCE_MC |
| 068H | 00H | Length in 256 byte units (MSB) | | | | | | | | | |
| 06AH | 21H | X | R | P | RO | A | T | | | X=0: no more misc fields<br>P=1: power-down supported<br>RO=0: read/write media<br>A=0: audio not supported<br>T=1: max twins is 1 | Miscellaneous features<br>TPCE_MI |
| 06CH | 1BH | CISTPL_CFTABLE_ENTRY | | | | | | | | Configuration tuple | Tuple code |
| 06EH | 06H | CISTPL_LINK | | | | | | | | Link length is 6 bytes | Link to next tuple |
| 070H | 00H | I | D | Configuration Index | | | | | | Memory mapped configuration index = 0 | TPCE_INDX |
| 072H | 01H | M | MS | | IR | IO | T | Power | | Power=1: $V_{CC}$ info, no $V_{PP}$ | TPCE_FS |
| 074H | 21H | R | DI | PI | AI | SI | HV | LV | NV | PI=1: peak current info<br>NV=1: nominal voltage info | TPCE_PD |
| 076H | B5H | X | Mantissa | | | | Exponent | | | X=1: extension byte present | |
| 078H | 1EH | X | Extension | | | | | | | Nominal voltage 3.30V | |
| 07AH | 4DH | X | Mantissa | | | | Exponent | | | Peak current 45 mA | |
| 07CH | 1BH | CISTPL_CFTABLE_ENTRY | | | | | | | | Configuration Tuple | Tuple code |
| 07EH | 0DH | CISTPL_LINK | | | | | | | | Link length is 13 bytes | Link to next tuple |
| 080H | C1H | I | D | Configuration Index | | | | | | I/O mapped, index=1<br>I=1: Interface byte follows<br>D=1:Default entry | TPCE_INDX |
| 082H | 41H | W | R | P | B | Interface type | | | | W=0: wait not required<br>R=1: ready/busy active<br>P=0: WP not used<br>B=0:BVD1, BVD2 not used<br>Type=1: I/O interface | TPCE_IF |
| 084H | 99H | M | MS | | IR | IO | T | Power | | M=1: misc info present<br>MS=0: no memory space info<br>IR=1: interrupt is used<br>IO=1: I/O space is used<br>T=0: no timing info specified<br>Power=1: $V_{CC}$ info, no $V_{PP}$ | TPCE_FS |
| 086H | 27H | R | DI | PI | AI | SI | HV | LV | NV | DI: no power-down current<br>PI=1: peak current info<br>AI: no average current info<br>SI: no static current info<br>HV=1: max voltage info<br>LV=1: min voltage info<br>NV=1: nominal voltage info | TPCE_PD |
| 088H | 55H | X | Mantissa | | | | Exponent | | | Nominal voltage 5.0V | |
| 08AH | 4DH | X | Mantissa | | | | Exponent | | | Minimum voltage 4.5V | |


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| Address | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 08CH | 5DH | X | Mantissa | | | | Exponent | | | Maximum voltage 5.5V | |
| 08EH | 75H | X | Mantissa | | | | Exponent | | | Peak current 80 mA | |
| 090H | 64H | R | S | E | IO | | | | | S=1: support 16 bit hosts<br>E=1: support 8 bit hosts<br>IO=4: address lines decoded | TPCE_IO |
| 092H | F0H | S | P | L | M | V | B | I | N | S=1: interrupt sharing logic<br>P=1:pulse mode supported<br>L=1:level mode supported<br>M=1: masks V..N present<br>V=0: no vendor unique IRQ<br>B=0: no bus error IRQ<br>I=0: no I/O check IRQ<br>N=0:no NMI | TPCE_IR |
| 094H | FFH | 1RQ7…0 | | | | | | | | Interrupt signal may be assigned to any host IRQ | |
| 096H | FFH | 1RQ15…8 | | | | | | | | | |
| 098H | 21H | X | R | P | RO | A | T | | | X=0: no more misc fields<br>P=1: power-down supported<br>RO=0: read/write media<br>A=0: audio not supported<br>T=1: max twins is 1 | TPCE_MI |
| 09AH | 1BH | CISTPL_CFTABLE_ENTRY | | | | | | | | Configuration Tuple | Tuple code |
| 09CH | 06H | CISTPL_LINK | | | | | | | | Link length is 6 bytes | Link to next tuple |
| 09EH | 01H | I | D | Configuration Index | | | | | | I/O mapped, index = 1 | TPCE_INDX |
| 0A0H | 01H | M | MS | | IR | IO | T | Power | | Power=1: $V_{CC}$ info, no $V_{PP}$ | TPCE_FS |
| 0A2H | 21H | R | DI | PI | AI | SI | HV | LV | NV | PI=1: peak current info<br>NV=1: nominal voltage info | TPCE_PD |
| 0A4H | B5H | X | Mantissa | | | | Exponent | | | X=1: extension byte present | |
| 0A6H | 1EH | X | Extension | | | | | | | Nominal voltage 3.30V | |
| 0A8H | 4DH | X | Mantissa | | | | Exponent | | | Peak current 45 mA | |
| 0AAH | 1BH | CISTPL_CFTABLE_ENTRY | | | | | | | | Configuration tuple | Tuple code |
| 0ACH | 12H | CISTPL_LINK | | | | | | | | Link length is 18 bytes | Link to next tuple |
| 0AEH | C2H | I | D | Configuration Index | | | | | | I/O mapped, index=2<br>I=1: Interface byte follows<br>D=1: Default entry | TPCE_INDX |
| 0B0H | 41H | W | R | P | B | Interface type | | | | W=0: wait not required<br>R=1: ready/busy active<br>P=0: WP not used<br>B=0:BVD1, BVD2 not used<br>Type=1: I/O interface | TPCE_IF |
| 0B2H | 99H | M | MS | | IR | IO | T | Power | | M=1: misc info present<br>MS=0: no memory space info<br>IR=1: interrupt is used<br>IO=1: I/O space is used<br>T=0: no timing info specified<br>Power=1: $V_{CC}$ info, no $V_{PP}$ | TPCE_FS |


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| Address | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0B4H | 27H | R | DI | PI | AI | SI | HV | LV | NV | DI: no power-down current<br>PI=1: peak current info<br>AI: no average current info<br>SI: no static current info<br>HV=1: max voltage info<br>LV=1: min voltage info<br>NV=1: nominal voltage info | TPCE_PD |
| 0B6H | 55H | X | Mantissa | | | | Exponent | | | Nominal voltage 5.0V | |
| 0B8H | 4DH | X | Mantissa | | | | Exponent | | | Minimum voltage 4.5V | |
| 0BAH | 5DH | X | Mantissa | | | | Exponent | | | Maximum voltage 5.5V | |
| 0BCH | 75H | X | Mantissa | | | | Exponent | | | Peak current 80 mA | |
| 0BEH | EAH | R | S | E | IO | | | | | R=1: range follows<br>S=1: support 16 bit hosts<br>E=1: support 8 bit hosts<br>IO=10: 10 lines decoded | TPCE_IO |
| 0C0H | 61H | LS | | AS | | NR | | | | LS=1: 1 byte length<br>AS=2: 2 byte address<br>NR=1: 2 address ranges | |
| 0C2H | F0H | Base address 1 (LSB) | | | | | | | | Address range 1<br>0x1F0 to 0x1F7 | |
| 0C4H | 01H | Base address 1 (MSB) | | | | | | | | | |
| 0C6H | 07H | Address range 1 length | | | | | | | | | |
| 0C8H | F6H | Base address 2 (LSB) | | | | | | | | Address range 2<br>0x3F6 to 0x3F7 | |
| 0CAH | 03H | Base address 2 (MSB) | | | | | | | | | |
| 0CCH | 01H | Address range 2 length | | | | | | | | | |
| 0CEH | EEH | S | P | L | M | IRQN | | | | S=1: interrupt sharing logic<br>P=1:pulse mode supported<br>L=1:level mode supported<br>M=0: masks V..N not present<br>IRQN=14: use interrupt 14 | TPCE_IR |
| 0D0H | 21H | X | R | P | RO | A | T | | | X=0: no more misc fields<br>P=1: power-down supported<br>RO=0: read/write media<br>A=0: audio not supported<br>T=1: max twins is 1 | TPCE_MI |
| 0D2H | 1BH | CISTPL_CFTABLE_ENTRY | | | | | | | | Configuration Tuple | Tuple code |
| 0D4H | 06H | CISTPL_LINK | | | | | | | | Link length is 6 bytes | Link to next tuple |
| 0D6H | 02H | I | D | Configuration Index | | | | | | I/O mapped, index=2 | TPCE_INDX |
| 0D8H | 01H | M | MS | | IR | IO | T | Power | | Power=1: $V_{CC}$ info, no $V_{PP}$ | TPCE_FS |
| 0DAH | 21H | R | DI | PI | AI | SI | HV | LV | NV | PI=1: peak current info<br>NV=1: nominal voltage info | TPCE_PD |
| 0DCH | B5H | X | Mantissa | | | | Exponent | | | X=1: extension byte present | |
| 0DEH | 1EH | X | Extension | | | | | | | Nominal voltage 3.30V | |
| 0E0H | 4DH | X | Mantissa | | | | Exponent | | | Peak current 45 mA | |


*This document, specifications and information herein are subject to change without notice.*

| Address | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0E2H | 1BH | CISTPL_CFTABLE_ENTRY | | | | | | | | Configuration tuple | Tuple code |
| 0E4H | 12H | CISTPL_LINK | | | | | | | | Link length is 18 bytes | Link to next tuple |
| 0E6H | C3H | I | D | Configuration Index | | | | | | I/O mapped, index=3<br>I=1: Interface byte follows<br>D=1: Default entry | TPCE_INDX |
| 0E8H | 41H | W | R | P | B | Interface type | | | | W=0: wait not required<br>R=1: ready/busy active<br>P=0: WP not used<br>B=0:BVD1, BVD2 not used<br>Type=1: Memory interface | TPCE_IF |
| 0EAH | 99H | M | MS | | IR | IO | T | Power | | M=1: misc info present<br>MS=0: no memory space info<br>IR=1: interrupt is used<br>IO=1: I/O space is used<br>T=0: no timing info specified<br>Power=1: $V_{CC}$ info, no $V_{PP}$ | TPCE_FS |
| 0ECH | 27H | R | DI | PI | AI | SI | HV | LV | NV | DI: no power-down current<br>PI=1: peak current info<br>AI: no average current info<br>SI: no static current info<br>HV=1: max voltage info<br>LV=1: min voltage info<br>NV=1: nominal voltage info | TPCE_PD |
| 0EEH | 55H | X | Mantissa | | | Exponent | | | | Nominal voltage 5.0V | |
| 0F0H | 4DH | X | Mantissa | | | Exponent | | | | Minimum voltage 4.5V | |
| 0F2H | 5DH | X | Mantissa | | | Exponent | | | | Maximum voltage 5.5V | |
| 0F4H | 75H | X | Mantissa | | | Exponent | | | | Peak current 80 mA | |
| 0F6H | EAH | R | S | E | IO | | | | | R=1: range follows<br>S=1: support 16 bit hosts<br>E=1: support 8 bit hosts<br>IO=10: 10 lines decoded | TPCE_IO |
| 0F8H | 61H | LS | | AS | | NR | | | | LS=1: 1 byte length<br>AS=2: 2 byte address<br>NR=1: 2 address ranges | |
| 0FAH | 70H | Base address 1 (LSB) | | | | | | | | Address range 1<br>0x170 to 0x177 | |
| 0FCH | 01H | Base address 1 (MSB) | | | | | | | | | |
| 0FEH | 07H | Address range 1 length | | | | | | | | | |
| 100H | 76H | Base address 2 (LSB) | | | | | | | | Address range 2<br>0x376 to 0x377 | |
| 102H | 03H | Base address 2 (MSB) | | | | | | | | | |
| 104H | 01H | Address range 2 length | | | | | | | | | |
| 106H | EEH | S | P | L | M | IRQN | | | | S=1: interrupt sharing logic<br>P=1:pulse mode supported<br>L=1:level mode supported<br>M=0: masks V..N not present<br>IRQN=14: use interrupt 14 | TPCE_IR |


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| Address | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 108H | 21H | X | R | P | RO | A | T | | | X=0: no more misc fields<br>P=1: power-down supported<br>RO=0: read/write media<br>A=0: audio not supported<br>T=1: max twins is 1 | TPCE_MI |


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# 21. REVISION HISTORY

| Revision | Date | Author | Notes |
|---|---|---|---|
| 1v0 | March 10, 2012 | HS | First Revision |
| 1v1 | March 6, 2014 | BR | Modified part numbers |

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