

Device	Company	Production Profile	Comments
NAND	Overall NAND	3D NAND transitions are finishing and they are slowing capacity adds	
	Samsung	85% 3D	<ul style="list-style-type: none"> - Transition from 64L QLC (quad-level cell) to 96L - Future investment in 2nd Xi'an fab, timing uncertain - Infrastructure spending continues, to address long-term demand
	SK Hynix	60% 3D	<ul style="list-style-type: none"> - Transition from 72L TLC (tri-level cell) to 96L QLC - Ramping production at M15; slower rate than initial plan - Expect net NAND wafers to decline; not adding capacity during transition
	Micron	90% 3D	<ul style="list-style-type: none"> - Transition from 64L QLC (quad-level cell) to 96L - No new fabs planned - 5% reduction in net wafers
	Toshiba	75% 3D	<ul style="list-style-type: none"> - Transition from 64L QLC (quad-level cell) to 96L - Planned expansion in 2020
	Intel	100% 3D	<ul style="list-style-type: none"> - Transition from 64L QLC (quad-level cell) to 96L - Starting Dalian Ph 2 production; limited 2019 NAND spending
	YMTC	100% 3D	<ul style="list-style-type: none"> - Ramp 32L production, transition to 64L in 2019 - Looking to jump to 128L in 2020
DRAM	Overall DRAM	Focus on node transitions; very limited capacity expansions.	
	Samsung	1x→1y nm	<ul style="list-style-type: none"> - Halted Pyeongtaek fab (Line 18) build-out, limits bit growth to ~20% YoY on transition to 1y nm technology.
	SK Hynix	1x→1y nm	<ul style="list-style-type: none"> - Forecasting bit growth mid- to high-teens - Focus on process and yield improvement
	Micron	1x ramp	<ul style="list-style-type: none"> - Forecasting bit growth mid- to high-teens - Investing for 1y transition in Taiwan and Japan; adding cleanroom capacity in both locations to support more process steps in 1y & 1z nodes - 5% reduction in net wafers
	JHICC	TBD	<ul style="list-style-type: none"> - Uncertain future on export ban on use of US technology
Foundry	Foundry/Logic	7nm ramp with EUV & Intel transition to 10nm support continued spending.	
	≤16nm	TSMC	<ul style="list-style-type: none"> - 7nm is underutilized. Will adjust future ramp plans. - 7+nm EUV production ramping starting 2Q'19, initial devices qualified - Announced 6nm half node shrink, based on 7nm (non-EUV) node
		Intel	<ul style="list-style-type: none"> - 14→10nm - 1H'18 high CPU demand driving high fab utilization & possible new CapEx - 10nm ramp must happen to plan in 2019 (esp. Israel) - Exiting 5G smartphone chip; limited impact to 2019 (CapEx, wafer starts) - Announced new fabs/expansions in Oregon & Israel (2020+)
		Samsung	<ul style="list-style-type: none"> - 7nm - 7nm EUV ramp expected to continue - Announced >\$100B investment through 2030; grow capability & capacity - Confirmed FinFET to 5nm but 3nm (~2025 volume) will be gate-all-around (GAA) requiring higher level of spending for new technology.
		GlobalFoundries	<ul style="list-style-type: none"> - 16nm - Initial 12nm transition to provide differentiation (vs. 16nm). - Sold old IBM East Fishkill plant to ON Semi; 4 year transition. Expect limited impact to SSB business. Sold 200mm VT fab to Marvell.
		UMC	<ul style="list-style-type: none"> - 16nm - Continue ramp of 16nm to have viable FinFET capability
		SMIC	<ul style="list-style-type: none"> - 16nm - Expecting to start 16nm production in Q1'19
	≥20nm	TSMC	<ul style="list-style-type: none"> - 28nm - 10% of 2019 spending for "specialty" chips (likely 200mm in Tainan)
		UMC	<ul style="list-style-type: none"> - 28nm - Limited activity, no announced plans for planar nodes
		SMIC	<ul style="list-style-type: none"> - 28nm - Limited activity, no announced plans for planar node
GlobalFoundries		<ul style="list-style-type: none"> - 28nm, FDSOI - Focus on FDSOI & 22nm transition to provide differentiation (vs. 28nm). 	